Transistor Level Implementation of CMOS Basic Gates in 0.18μm Technology

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Abstract
This paper presents a technique for creating CMOS combinational circuits using MOSFET transistors. The MOSFET is very important part of Digital Integrated Circuits. It is mostly used as switch in digital design. The material presented is suitable for use in an introductory circuit’s course. The NMOS and PMOS transistors are approximated as ideal switches. This paper deals with the design of some basic gate and transistor-level simulations using DSCH 3.1 and Microwind3.1 CAD tool.

Keywords
VLSI, CMOS, CMOS basics gates

I. INTRODUCTION

VLSI design is a modular methodology for saving microchip area by minimizing the interconnect fabrics and to increase circuit efficiency in terms of complexity of circuit, power consumption and frequency response associated to the design. Logic chip such as microprocessor chip and digital signal processing chips contains large array of memory cell and different functional unit. Hence their design complexity is considered much higher than memory chip, the level of circuit performance depend on the efficiency of the design methodology and design style.

The choice of the design style for a VLSI product depend on the performance requirement, the technologies being used, lifetime of product and the cost of the project. The Metal Oxide Semiconductor Field Effect Transistor is very important part of Digital Integrated Circuits. It is mostly used as switch in digital design. MOSFET is a four terminal device. The voltage applied to the gate terminal determine the current flow between drain and source terminals. The body/substrate of the transistor is the fourth terminal. Mostly the fourth terminal (body/substrate) of the device is connected to dc supply that is identical for all devices of the same type (GND for NMOS and Vdd for PMOS). Usually this terminal is not shown on the schematics.

The NMOS transistor consists of n+ drain and source diffusion regions, which are embedded in a p-type substrate. The electrons in the channel beneath the gate between source and drain terminal are responsible for the current flow. The PMOS transistor consists of p+ drain and source diffusion regions, which are embedded in an n-type substrate. The holes in the channel beneath the gate between source and drain terminal are responsible for the current flow. This paper discusses the design of CMOS basic gates and their simulation result.
II. CMOS LOGIC GATE CONCEPT

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material.

CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits found in computers, telecommunications equipment, and signal processing equipment. Although CMOS logic can be implemented with discrete devices (e.g., for instructional purposes in an introductory circuits class), typical commercial CMOS products are integrated circuits composed of millions of transistors of both types on a rectangular piece of silicon of between 10 and 400mm². These devices are commonly called "chips". The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion; N diffusion for the N device & P diffusion for the P device. The output is connected together in metal. Connections between metal and polysilicon or diffusion are made through contacts.

The N device is manufactured on a P-type substrate while the P device is manufactured in an N-type well (n-well) as shown in figure 1. A P-type substrate "tap" is connected to V_SS and an N-type n-well tap is connected to V_DD to prevent latch up.

Fig.1 Cross Section of Two Transistor In CMOS

III. DESIGN OF CMOS GATE

In CMOS designs, two transistor structures (one pmos and one nmos) are required for implementing the functional expression. In logic systems, the analogous expression defines what is required to generate the required output assertion level. The complementary expression, obtained by applying DeMorgan's theorem to the functional expression, defines the complementary structure. These two expressions, the analogous and the complementary,
are then used to create the transistor network for a CMOS circuit. The design procedure is described as follows in five steps.

i) Identify the "most common" input level by examination of the input assertion levels. This requires that the input assertion levels be defined. An input variable containing a conflict is treated as if it has the opposite assertion level. The "most common" input level will be either "Low" or "High". This is determined by counting the number of asserted high or asserted low inputs after adjusting for conflicted inputs.

ii) The "most common" input level is used to specify the type of transistors used for implementing the analogous structure.

iii) If there is not a "most common" input level then select the input level to be the opposite level of the required output assertion level.

iv) a) Create the analogous transistor structure directly from the functional logic expression. Use the transistor type specified in part 2 for creating the structure.

(b) The complementary structure is created by applying DeMorgan's theorem to the analogous expression.

v) Assemble the analogous and complementary structures to create the full CMOS equivalent circuit. In some cases, an inverter must be added to the output of the circuit to correct the output assertion level.

Fig. 2 General Structure of CMOS Basic Gate

Using complementary pairs of NMOS and PMOS devices, either the lower NMOS network is active, which ties the output to ground; either the upper PMOS network is active, which ties the output to VDD.

1. CMOS NAND GATE

In CMOS design, the NAND gate consists of two NMOS in series connected to two PMOS in parallel. The schematic diagram of the CMOS NAND cell is reported below. The NMOS devices in series tie the output to the ground for one single combination A=1 and B=1. For the three other combinations, the NMOS path is cut, but at least one PMOS ties the output to the supply VDD. Notice that both NMOS and PMOS devices are used in their best regime: the NMOS devices pass "0", the PMOS pass "1". The circuit of CMOS NAND gate is as shown in figure 3.
Table 1 shows the truth table for CMOS NAND gate.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>NMOS</th>
<th>PMOS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
<td>On</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
<td>On</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Off</td>
<td>On</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>On</td>
<td>Off</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1 Truth table of CMOS NAND gate

2. CMOS NOR GATE

In CMOS design, the NOR gate consists of two NMOS in parallel connected to two PMOS in series. The NMOS in parallel tie the output to the ground if either A or B are at 1. When both A and B are at 0, the NMOS path is cut, but the two PMOS devices in series tie the output to the supply VDD. The schematic of CMOS NOR gate is as shown in figure 4.
Table 2 shows the truth table for CMOS NOR gate.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>NMOS</th>
<th>PMOS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
<td>On</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>On</td>
<td>Off</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>On</td>
<td>Off</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>On</td>
<td>Off</td>
<td>0</td>
</tr>
</tbody>
</table>

Table.2 Truth table of CMOS NOR gate

IV. SIMULATION AND RESULTS

Figure 5 shows the result of CMOS NAND gate having power consumption 11.168 μW and delay 12ps.

![Fig. 5 Waveform of cmos nand gate](image)

Figure 6 shows the result of CMOS NOR gate having power consumption 9.385 μW and delay 14ps.

![Fig. 6 Waveform of cmos nor gate](image)
V. Comparison of Gate

Comparison of NAND and NOR gate on the basis of power and delay is as shown in table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NAND</th>
<th>NOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>11.168μW</td>
<td>9.385μW</td>
</tr>
<tr>
<td>Delay</td>
<td>12Ps</td>
<td>14Ps</td>
</tr>
<tr>
<td>current</td>
<td>0.440mA</td>
<td>0.179mA</td>
</tr>
</tbody>
</table>

Table 3. Comparison of NAND & NOR gate

From table it is clear that implementation of NOR gate gives low power consumption as compared to the NAND gate though it has less delay.

VI. Conclusion

In this work, circuits NAND and NOR are successfully implemented using CMOS logic in DSCH 3.1 and Microwind3.1 CAD tool. Considering the parameter power-delay each of the circuits is compared. NOR gate consumes less power hence it can be used in the implementation of various circuit.

VII. REFERENCES


