A NOVEL DESIGN AND IMPLEMENTATION OF MTCMOS BASED LOW POWER D-LATCH

T. Krishna Moorthy[#1], K. Neelima[#2], K. S. Chakradhar[#3]

[#1]Assistant Professor, SVEC (Autonomous), Tirupati, Andhra Pradesh,
Ph.no.: 9396828334,
[#2]Assistant Professor, SVEC (Autonomous), Tirupati, Andhra Pradesh,
Ph.no.: 9966547895,
[#3]Associate Professor, SVEC (Autonomous), Tirupati, Andhra Pradesh,
Ph.no.:9490089654,

ABSTRACT

As technology is scaled down, within less area many transistors are integrated. Along with the main circuits designed, the latches and flip-flops are also required for the storage of memory bits. To maintain proper speed of the chip as a whole, some transistors have to be slowed down by varying the threshold voltage of the device. This paper proposes a low power, high speed latch with minimum number of transistors designed with TSPC and MTCMOS. Based on power consumption, propagation delay, using DSCH and Microwind tools, the PDP for different technologies are calculated and compared. MTCMOS based 5T D-Latch is found to have 45% decrease in power dissipation.

Keywords: Threshold Voltage, Latch, TSPC, MTCMOS, PDP.

INTRODUCTION

A Latch is a data storage element capable of storing a logic state either 0 or 1, used as basic storage element in sequential logic. Latches are used as fundamental building blocks in digital electronics based on system used in computer, communication between the devices. D-Latch forms the basic latch called as delay or data latch used to propagate the input based on device enable signal.

In CMOS[1][5] circuits the combination of PMOS and NMOS is used which have different delays and power consumption. The threshold voltage, Vth, of a MOSFET is usually defined as the gate voltage at which an inversion layer is formed at the interface between the insulating or oxide layer and the substrate of the transistor, i.e., the gate voltage for which the device turns on. The threshold voltage can be modified by varying the body effect parameter, the choice of oxide and the oxide thickness[4][7].

Multi-threshold CMOS (MTCMOS) is a traditional method of low power design used to optimize delay, area and power i.e., a variation of CMOS chip technology. As Low threshold devices switch faster, they are used in critical delay paths i.e., for logic devices to minimize clock periods but these lead to higher static leakage power. Similarly High threshold devices are used in non-critical paths i.e., these are used as sleep transistors to reduce static leakage power around ten times typically, without any penality in delay.

There are different methods to create devices with multi-threshold voltage values like different bias voltages can be applied to the substrate of the MOSFET device, by adjusting the gate oxide thickness, or gate oxide dielectric constant i.e., the material type, or dopant concentration in the channel region of the transistor. Multi-threshold CMOS

devices can be fabricated by adding additional steps like ion implantation, photolithography, etc.

This paper is organized as the discussion on previous technique in section-II. Section-III gives the details about the proposed MTCMOS based D-Latch and its functionality. Section-IV gives details about the simulation results and comparison. Section-V concludes the paper.

TSPC BASED D-LATCH

True Single Phase Clocked (TSPC)[2][3] Latch is used to reduce the number of transistors and clock load by 50%, to lower the voltage swing at the nodes for V_{in} =0 (Logic '0'). Fig.1 shows the schematic of TSPC D-Latch using six transistors (6T) and fig.2 shows the developed layout for 6T TSPC D-Latch for 90nm technology.

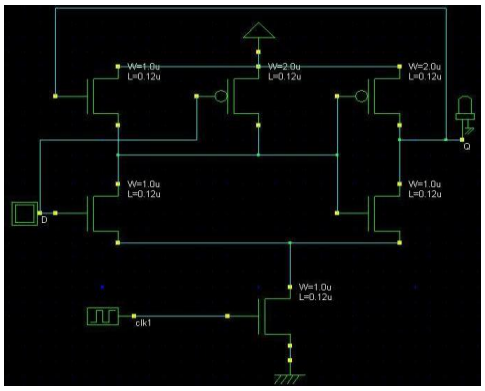

Fig 1: Schematic of 6T TSPC D-Latch

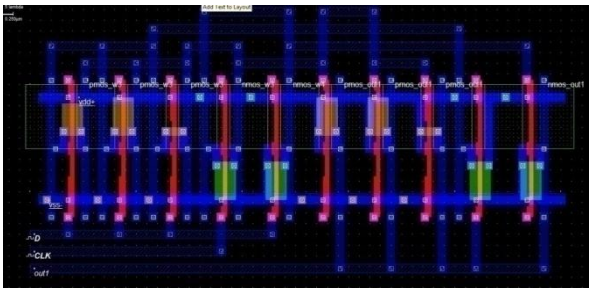

Fig 2: Layout of TSPC 6T D Latch

Table.1 represents the truth table of 6T TSPC D-Latch, which represents the switching of the transistors present in the design and the arrow for the clock in upward direction indicates the transition of clock signal from logic '0' to logic '1'. Similarly, the arrow indicated downwards indicates the logic transition of clock signal from logic '1' to logic '0'.

Table 1. Truth Table of 6T TSPC D-Latch

CLK	IN	M1	M2	M3	M4	M5	M6	OUT
↑	0	OFF	OFF	ON	OFF	OFF	ON	0
↑	1	ON	ON	OFF	ON	ON	OFF	1
↓	0	OFF	OFF	ON	OFF	0FF	ON	0
↓	1	ON	OFF	OFF	OFF	OFF	OFF	0

The TSPC Latches can be developed by using five transistors as shown in fig.3. In this design a input is connected to both PMOS and NMOS device for proper logic switching. Fig.4 shows the developed layout for 5T TSPC D-Latch for 90nm technology.

Issue 2 volume 4, August 2012
ISSN 2249-9954

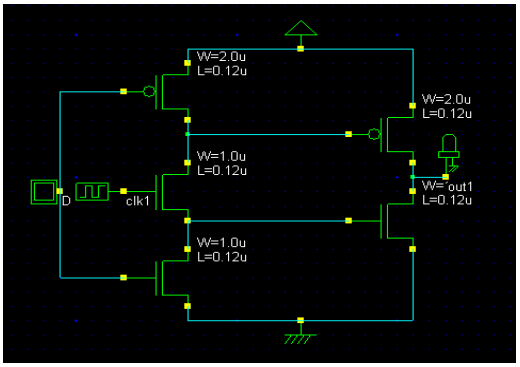

Fig 3: Schematic of 5T TSPC D-Latch

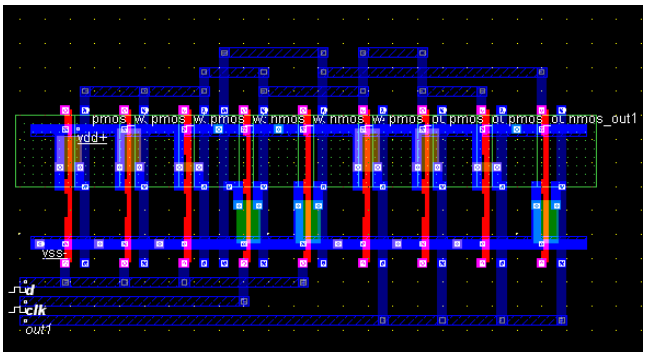

Fig 4: TSPC 5T D Latch Layout

Table.2 represents the truth table of 5T TSPC D-Latch, which represents the switching of the transistors present in the design and their operation. The arrows for the clock are similar to that described above.

Table 2. Truth Table of 5T D-Latch

CLK	IN	M1	M2	M3	M4	M5	OUT
↑	0	ON	ON	OFF	OFF	ON	0
↑	1	OFF	ON	ON	ON	OFF	1
↓	0	ON	OFF	OFF	OFF	OFF	0
↓	1	OFF	OFF	ON	OFF	OFF	0

MTCMOS BASED D-LATCH

Multi-threshold CMOS[6][8] is a traditional technique which enables low power, high performance operation. As the sequential circuit structures can retain state during standby modes, this method is well suited for Latches and Flip-Flops design. The efficient MTCMOS based Latch utilizes sleep and sleep bar transistors to retain state of the Latch during standby modes.

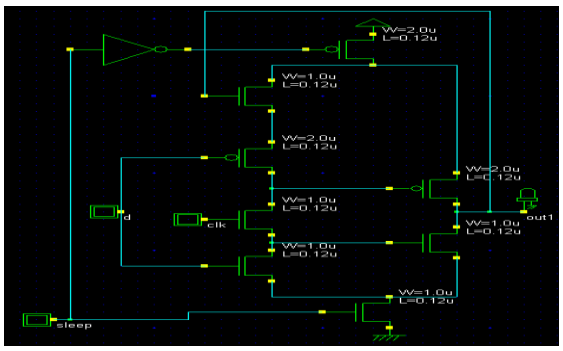

Fig 5: Schematic of 6T MTCMOS D-Latch

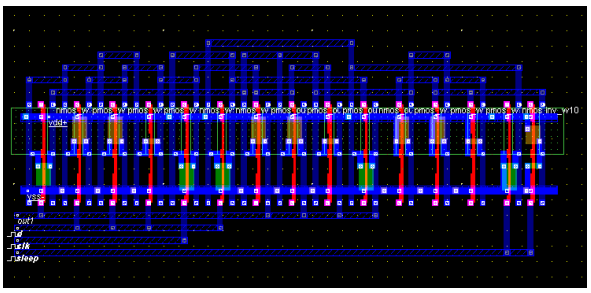

Fig 6: Layout of MTCMOS 6T D Latch

The Table.3 shows the truth table of 6T MTCMOS D-Latch. For example consider the input is '1' and sleep input is '1', then for a rising clock input, the transistors are turned on correspondingly to produce a logic '1' output.

Table 3. Truth Table of 6T MTCMOS D-Latch

CLK	IN	Sleep	M1	M2	M3	M4	M5	M6	M7	M8	OUT
↑	0	0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	0
↑	0	1	ON	ON	OFF	OFF	OFF	OFF	ON	ON	0
↑	1	0	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	0
↑	1	1	OFF	ON	ON	ON	ON	OFF	ON	ON	1
↓	0	0	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	0
↓	0	1	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	0
↓	1	0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	0
↓	1	1	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	0

As the design has to be compact and well suited for any technology, the number of transistors used here for the design of D-Latch is reduced from six to five for the same function as shown in fig.7 and the corresponding truth table is shown in table.4. The developed layout for 90nm technology is shown in fig.8.

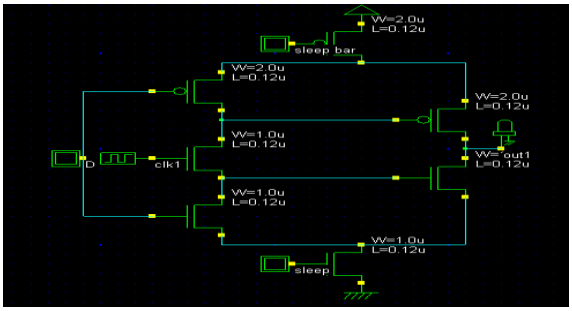

Fig 7: 5T MTCMOS D-Latch

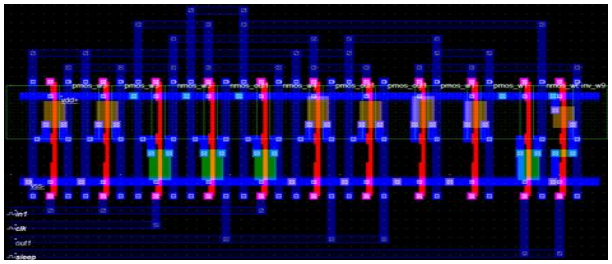

Fig 8: Layout of MTCMOS 5T D Latch

Table 4. Truth Table for 5T MTCMOS D-Latch

CLK	IN	Sleep	M1	M2	M3	M4	M5	M6	M7	OUT
↑	0	0	ON	ON	OFF	OFF	ON	ON	OFF	0
↑	0	1	ON	ON	OFF	OFF	OFF	OFF	ON	0
↑	1	0	OFF	ON	ON	ON	OFF	ON	OFF	1
↑	1	1	OFF	ON	ON	ON	OFF	OFF	ON	1
↓	0	0	ON	OFF	OFF	OFF	OFF	ON	OFF	0
↓	0	1	ON	OFF	OFF	OFF	OFF	OFF	ON	0
↓	1	0	OFF	OFF	ON	OFF	OFF	ON	OFF	0
↓	1	1	OFF	OFF	ON	ON	OFF	OFF	ON	0

Issue 2 volume 4, August 2012
ISSN 2249-9954

RESULTS AND DISCUSSION

The simulated waveforms of the D-Latch using TSPC and MTCMOS are shown in fig.10 and fig.11 respectively. The output responses show that the waveforms are appropriate for MTCMOS based design when compared to TSPC based design.

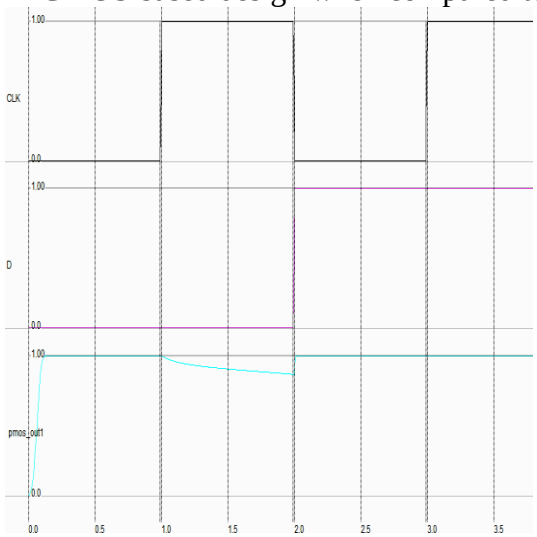

Fig 10: Simulation Output of 5T TSPC D-Latch

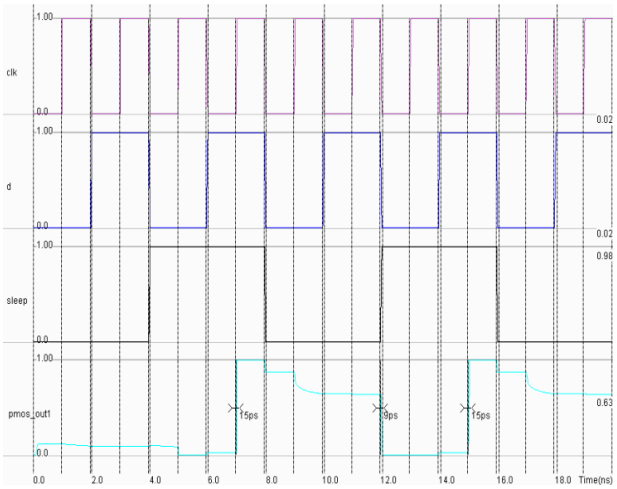

Fig 11: simulation Output of 5T MTCMOS D-Latch

The tables 5 and 6 show the details of measured power dissipation in µW and delay in ns for six transistors and five transistors based TSPC and MTCMOS based D-Latch.

Table 5. Power Delay Comparison for 6T TSPC and MTCMOS based D Latch

Parameters	90nm				70nm				50nm			
	0.5V		1V		0.5V		1V		0.5V		1V	
	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS
Power Dissipation (µw)	0.90	1.929	21.47	2.52	1.023	0.360	30.47	2.32	0.74	0.450	36.62	2.12
Delay(ns)	0.049	0.649	0.016	0.994	0.043	0.750	0.080	0.510	0.045	0.675	0.013	0.543
Power Delay Product (fj)	0.044	1.249	0.34	2.213	0.43	0.27	2.43	1.224	0.033	0.307	0.47	1.151

Table 6. power delay comparison for TSPC and MTCMOS based 5T D Latch

Parameters	90nm				70nm				50nm			
	0.5V		1V		0.5V		1V		0.5V		1V	
	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS	TSPC	MTCMOS
Power Dissipation (µw)	2.12	0.514	2.953	1.97	2.67	0.473	3.15	1.837	2.893	0.280	4.11	1.173
Delay(ns)	0.130	0.142	0.147	0.142	0.144	0.236	0.104	0.23	0.143	0.370	0.079	0.236
Power Delay Product (fj)	0.275	0.0729	0.434	0.28	0.384	0.111	0.327	0.42	0.413	0.104	0.324	0.277

From the tables 5 and 6, it is clear that the power dissipation decreases and propagation delay increases as the technology is scaled down. Also as the supply voltage is scaled down, both the power dissipation and propagation delay decrease. When compared with TSPC based D Latch, the MTCMOS based D Latch has advantage of low power delay product which is well suited for high performance applications.

CONCLUSION

MTCMOS technique based Latches have less power consumption compared to the TSPC based Latches, as the transition of signals is controlled by the extra two transistors, i.e., sleep and sleep bar transistors which reduces the dynamic power dissipation. From results, as the technology is scaled down power dissipation decreases and propagation delay increases. From the details of Figure of merit MTCMOS based Flip- Flop has least power delay product, which gives rise to best performance The MTCMOS technique reduces 80% of the leakage power compared TSPC technique. Hence, the circuits designed using MTCMOS are suitable for high performance applications like level converters, microprocessors, clocking systems counters, etc.

REFERENCES

[1] M. A. Hernandez and M. L. Aranda, "A Clock Gated Pulse –Triggered D Flip-Flop For Low Power High Performance VLSI Synchronous Systems," Proceedings of the 6th International Caribben Conference on devices, circuits and systems, Mexico, Apr. 26-28, 2006.

[2] J. Wang et al., "Design of a 3-V 300-MHz Low-Power 8-b ×8-b Pipelined Multiplier Using Pulse-Triggered TSPC Flip Flops," IEEE J. Solid-State Circuits, vol. 35, no. 5, pp. 583-591, Apr. 2000.

[3] J.S. Wang, P.H. Yang "A Pulse Triggered TSPC FF for high speed, low power VLSI design applications" IEEE, 1998.

[4] A. Keshavarzi, K. Roy, and C. F. Hawkins, "Intrinsic leakage in low power deep submicron CMOS ics," in Proc. Int. Test Conf., pp. 146– 155, 1997.

[5] S.M. Kang, Y. Leblebici "CMOS Digital Integrated Circuits analysis and design" third edition, TMH, 2003.

[6] J.T. Kao et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE J. Solid-State Circuits, vol. 35, no. 7, pp. 1009- 1018, July 2000.

[7] N. Sirisantana, L. Wei, and K. Roy, "High- Performance Low-Power CMOS Circuits Using Multiple Channel Length and Multiple Oxide Thickness," Proc. Int'l Conf. Computer Design (ICCD '00), IEEE CS Press, pp. 227-234, 2000.

[8] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices. New York: Cambridge Univ. Press, ch. 2, pp. 94–95, 1998.