Quasi-Active Power Factor Correction of A High-Efficiency AC/DC Converter

Miriyala Tharunkumar[1], Abid Nayeemuddin[2]

[1](PG *Student Department of Electrical & Electronics Engineering, G.Pullareddy Engineering College, Andrapradesh, India*
[2](*Assistant professor, Department of Electrical & Electronics Engineering, G.Pullareddy Engineering College, Andrapradesh, India)*

ABSTRACT
This letter presents a novel ac/dc converter based on a quasi-active power factor correction (PFC) scheme. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc flyback converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. In order to achieve low harmonic content, the input inductor is designed to operate in discontinuous current mode. Operating principles, analysis, and experimental results of the proposed method are presented.

Index Terms— AC/DC converter, power factor correction, single stage**.**

I. INTRODUCTION

Conventional offline power converters with diode–capacitor rectifiers have resulted in distorted input current waveforms with high harmonic contents. To solve these problems, so as to comply with the harmonic standards such as IEC 61000-3-2, several techniques have been proposed to shape the input current waveform of the power converter. A common approach to improving the power factor is a two-stage power conversion approach. The two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed [1]–[11]. These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation. Usually, the DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields slightly higher efficiency compared to the DCM operation. A detailed review of the single stage PFC converters is presented in [3].

Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they
do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation. In addition, although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and high as well as wide-range intermediate dc bus voltage stress [5], [6]. To overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented [3]–[12], in which a high frequency ac voltage source (dither signal) is connected in series with the rectified input voltage in order to shape the input current (see Fig. 1). Another technique based on parallel connection of this dither signal is presented in [13], however, the harmonic content can meet the regulatory standard by a small margin. In [14], a new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values.

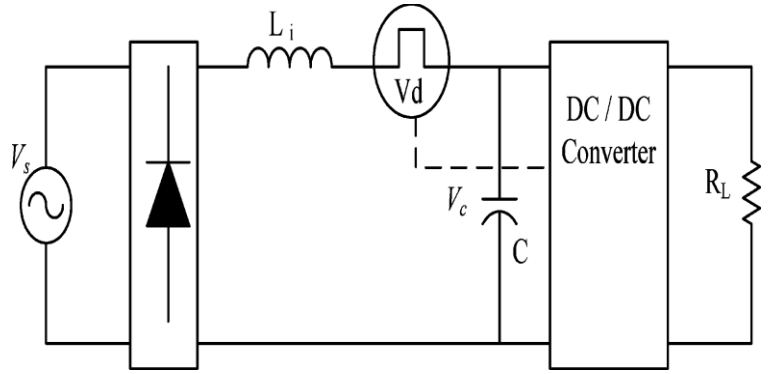


Fig. 1. General circuit diagram of dither rectifier with PFC cell.

In this letter, a new technique of quasi-active PFC is proposed. As shown in Fig. 2, the PFC cell is formed by connecting the energy buffer (*LB)* and an auxiliary winding (*L*3) coupled to the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current

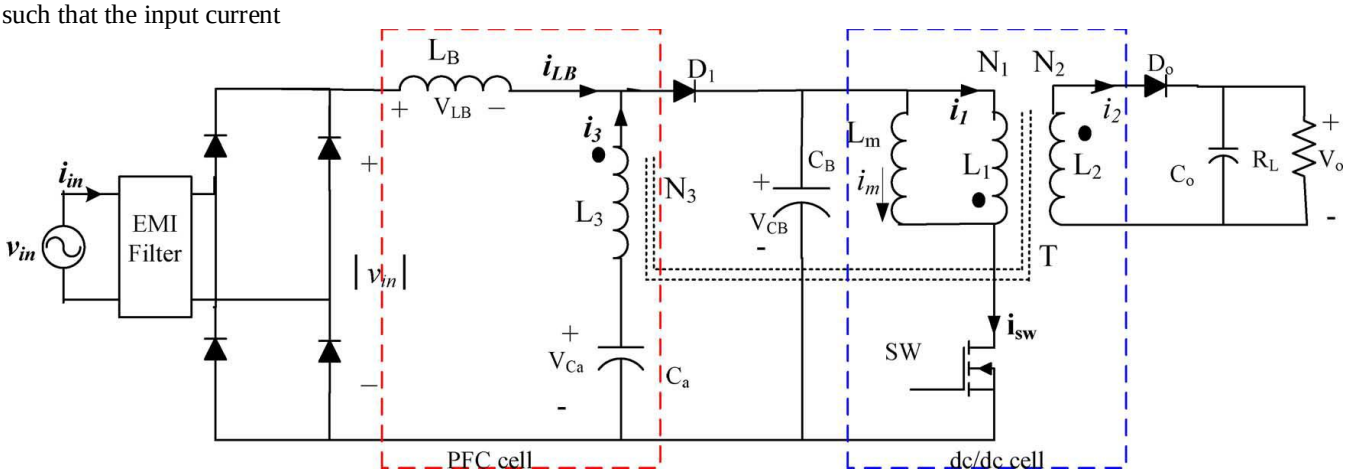


Fig. 2. Proposed quasi-active PFC circuit diagram

conduction angle is significantly lengthened and the input current harmonics is reduced. The input inductor *LB* operates in DCM such that a lower THD of the input current can be achieved. The structure, operation principles, and analysis of the proposed converter are presented in Section II. Design example and the experimental results are presented in Section III.

II. PROPOSED QUASI-ACTIVE PFC CIRCUIT

The proposed quasi-active PFC circuit is analyzed in this section. As shown in Fig. 2, the circuit comprised of a bridge rectifier, a boost inductor *LB*, a bulk capacitor *Ca* in series with the auxiliary windings *L*3, an intermediate dc-bus voltage capacitor *CB*, and a discontinuous input current power load, such as flyback converter. The flyback transformer (*T*) has three windings *N*1, *N2*, and *N*3. The secondary winding *N*2 = 1is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high-frequency pulsating source. The quasiactive PFC cell can be considered one power stage but without an active switch.

To simplify the analysis, the following assumptions have been made.

1) All semiconductors components are ideal. According to this assumption, the primary switch and the rectifiers do not have parasitic capacitances and represent ideal short and open circuits in their ON and OFF states, respectively.
2) The power transformer does not have the leakage inductances because of the ideal coupling.
3) All the capacitors are high enough so that the voltage across them is considered constant.
4) Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line frequency.

A. Principles of Operation of the Proposed Circuit

To facilitate the analysis of operation, Fig. 3(a) and (b) shows the topological stages and the key waveforms of the proposed circuit. It is assumed that both the input inductor

LB and the magnetizing inductance of the flyback converter operate in DCM. Therefore, currents *iLB* , *im*, and *i*2 are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage *VCa* is greater than the average rectified input voltage |*v*in |. To ensure proper operation of the converter, the transformer's turns ratio should be (*N*1/*N*3) ≥ 2 and the boost inductor *LB* < *Lm*. In steady-state operation, the topology can be divided into four operating stages.

*1) Stage 1 (to − t*1)*:* When the switch (SW) is turned on at *t = to*, diodes *D*1 and *Do* are OFF, therefore, the dc-bus voltage *VCB* is applied to the magnetizing inductor *Lm*, which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{V_{CB}}{L_m}(t_0 - t_1) \qquad (1)$$

And since diode *D*1 is OFF, the input inductor L_B is charged by input voltage; therefore, the inductor current i_{LB} is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as

$$i_{LB} = \frac{|V_{in}| + \left(N_3/N_1\right)V_{CB} - V_{Ca}}{L_B}(t_0 - t_1) \qquad (2)$$

Where, *V*in = *Vm*| sin *θ*| is the rectified input voltage, (*to* − *t*1) = *dTS* is the ON-time of the switch (SW), *LB* is the boost inductor and *N*1, *N*3 are the primary and auxiliary turns ratio, respectively. At this stage, *iLB* = −*i*3 and the capacitor
Ca is in the charging mode. On the other hand, *Do* is reversed biased and there is no current flow through the secondary winding. Since the transformer is assumed ideal, based on Ampere's law, it has

$$N_1 i_1 + N_2 i_2 - N_3 i_{LB} = 0$$

Where *i2* = 0 at this stage therefore,

$$i_1 = \frac{N_3}{N_1} i_{LB} = -\frac{N_3}{N_1} i_3 \qquad (3)$$

Thus

$$i_m = i_{CB} - i_1 = i_{CB} + \frac{N_3}{N_1} i_3 \qquad (4)$$

Therefore, from (4) it can be seen that the magnetizing current *im* is supplied by the discharging current from the dc bus capacitor *CB* and the current *i*3 which is equal to input current *iLB* at this stage. The current through the main switch (SW) is given by

$$i_{SW} = i_{CB} = i_m - \frac{N_3}{N_1} i_3 = i_m + \frac{N_3}{N_1} i_{LB} \qquad (5)$$

Therefore, the current stress of the switch can be reduced by
selecting the turns ratio (*N*3/*N*1), which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter [11], the switch current is given by

$$i_{SW} = i_m + i_{LB} \qquad (6)$$

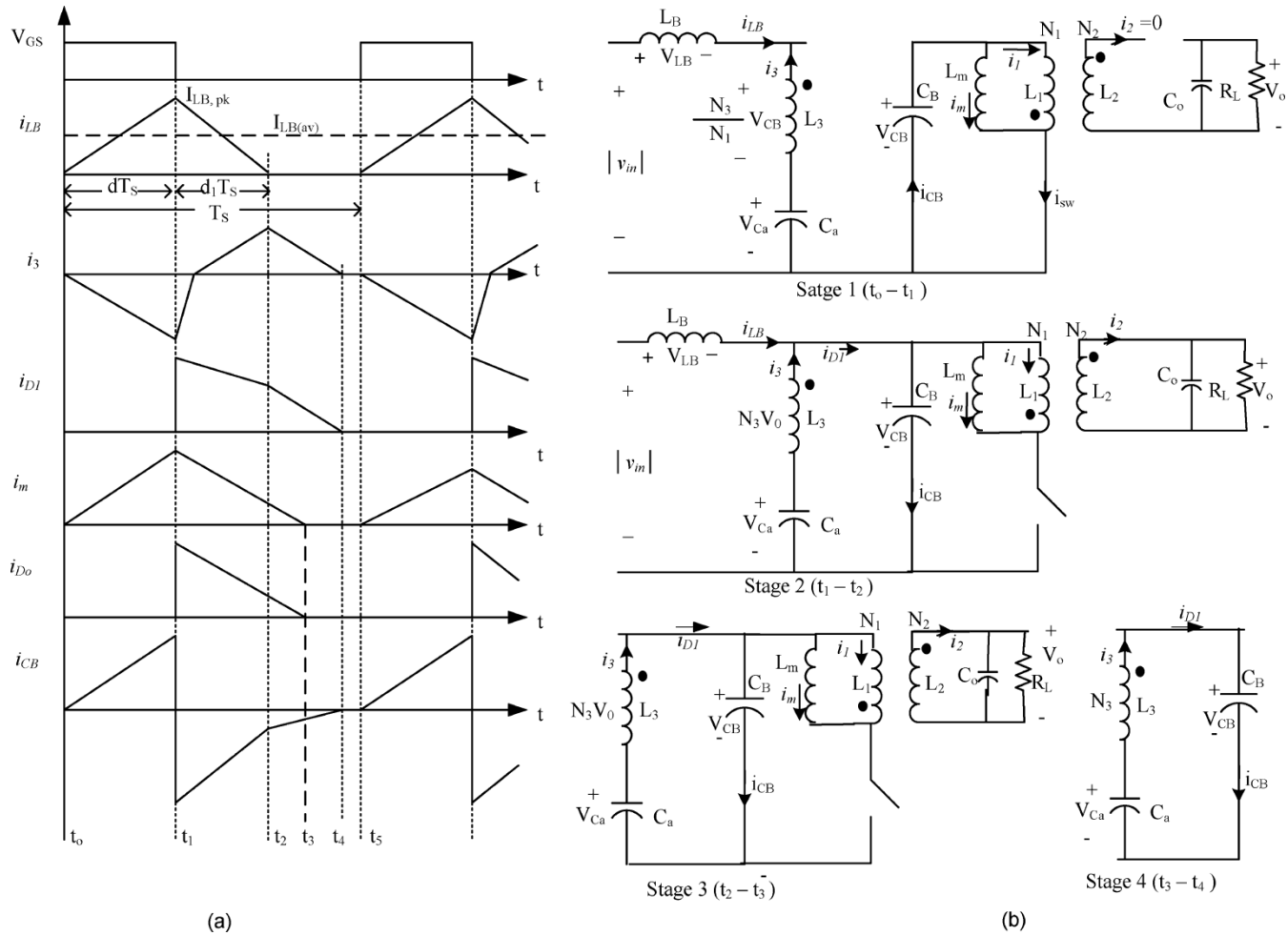


Fig. 3. (a) Key switching waveforms of the proposed PFC. (b) Equivalent circuit operation stages of the proposed PFC circuit during one switching period.

Obviously, the proposed circuit has less switch current stress, therefore, the conduction loss and switching losses are reduced, and the efficiency is improved correspondingly. This stage ends when the switch is turned off at $t = t1$.

2) Stage 2 ($t1 - t2$*):* When the switch is turned OFF at $t = t1$, output diode *Do* begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. Similarly, the diode *D*1 is also forward biased and the voltage across *LB* now *V*in − *VCB*. Therefore, the current *ILB* is linearly decreased to zero at $t = t2$ (DCM operation), and the energy stored in *LB* is delivered to the dc bus capacitor *CB*. Therefore

$$i_{LB} = \frac{|V_{in}| - V_{CB}}{L_B}(t_1 - t_2) \quad (7)$$

The capacitor (*Ca)* is also discharging its energy to the dc buscapacitor *CB* and the current *i*3 reverse its direction. Therefore,the capacitor current is given by

$$i_{D1} = i_{CB} = i_{LB} + i_3 \quad (8)$$

3) Stage 3 ($t2 - t3$ *):* At this stage, the input inductor current *iLB* reaches zero and the capacitor *Ca* continues to discharge its energy to the dc bus capacitor *CB* . Therefore, $iD1 = iCB = i3$ .At $t = t3$, the magnetizing inductor

releases all its energy to the load and the currents *im* and *i*2 reach to zero level because a DCM operation is assumed.

*4) Stage 4 (t*3 − *t*4 *):* This stage starts when the currents *im* and *i*2 reach to zero. Diode*D*1 still forward biased, therefore, the capacitor *Ca* still releasing its energy to the dc bus capacitor *CB* . This stage ends when the capacitor *Ca* is completely discharged and current *i*3 reaches zero. At *t* = *t*5 the switch is turned on again to repeat the switching cycle.

B. Steady-State Analysis

The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors andthe input–output power balance as explained in the following. From the volt-second balance on *LB*

$$\left(V_{in}+\frac{N_3}{N_1}V_{CB}-V_{Ca}\right)dT_s=\left(V_{CB}-V_{in}\right)d_1T_s \quad (9)$$

where *d*1 is the OFF-time of the switch (SW). Therefore, *d*1 could be given by

$$d_1=\frac{V_{in}+\left(N_3/N_1\right)V_{CB}-V_{Ca}}{V_{CB}-V_{in}}d \quad (10)$$

From Fig. 3(a), the average current of the boost inductor in a switching cycle is given by

$$I_{in}=I_{LB,av}=\frac{i_{LB,Peak}}{2}\left(d+d_1\right)T_s \quad (11)$$

Substituting for *iLB,*peak given in (2) and using (10), the average input current is given by

$$I_{in}=\frac{V_{in}+\left(N_3/N_1\right)V_{CB}-V_{Ca}}{2L_B}d^2T_s\times\left(\frac{\left(1+N_3/N_1\right)V_{CB}-V_{Ca}}{V_{CB}-V_{in}}\right) \quad (12)$$

Based on (12) for a given input voltage, Fig. 4(a) shows the normalized input current waveform in a half cycle for a change in the turns ratio *N*3/*N*1 . It can be seen that to reduce the dead time and improve the power factor of the input current the turns ratio must be ≥0.5. Similarly, Fig. 4(b) shows the normalized input current waveform for a change in dc bus capacitor voltage *VCB*. As it can be seen that the higher the *VCB* the better quality of the input current waveform (lower THD). However, higher *VCB* means higher voltage stress on the power switch (SW), which can reduce the efficiency of the converter. Therefore, a tradeoff between THD and efficiency must be made.

The energy absorbed by the circuit from the source during a half switching cycle is given by

$$P_{in}=\frac{1}{\pi}\int_0^{\pi}V_m\sin(t)I_{in}dt$$

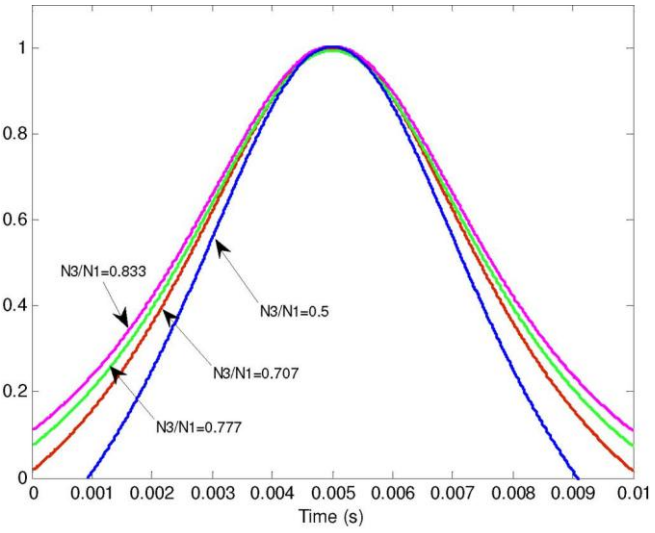
Substation for I_{in} in given (12) yields

$$P_{in}=\frac{1}{\pi}\frac{V_m}{2L_B}d^2T_s\left(A\right)\int_0^{\pi}\sin(t)Bdt \quad (13)$$

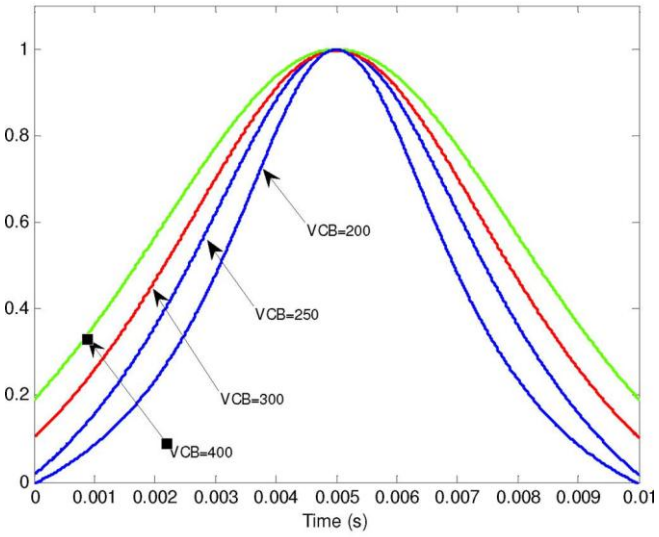
Where

$$A = \left[\left(1 + {}^{N_3}\!/_{N_1}\right)V_{CB} - V_{Ca}\right]$$

$$B = \frac{V_m \sin(t) + \left({}^{N_3}\!/_{N_1}\right)V_{CB} - V_{Ca}}{V_{CB} - V_m \sin(t)}$$



(a)



(b)

Fig. 4. Normalized input current waveform in half cycle for a change in (a) turns ratio *N*3/*N*1 and (b) bus capacitor voltage *VCB*.

The average output power for a DCM flyback converter is given by

$$P_0 = \frac{V_{CB}^2}{2L_m} d^2 T_s \qquad (14)$$

Equation (15) shows that the dc bus capacitor is independent

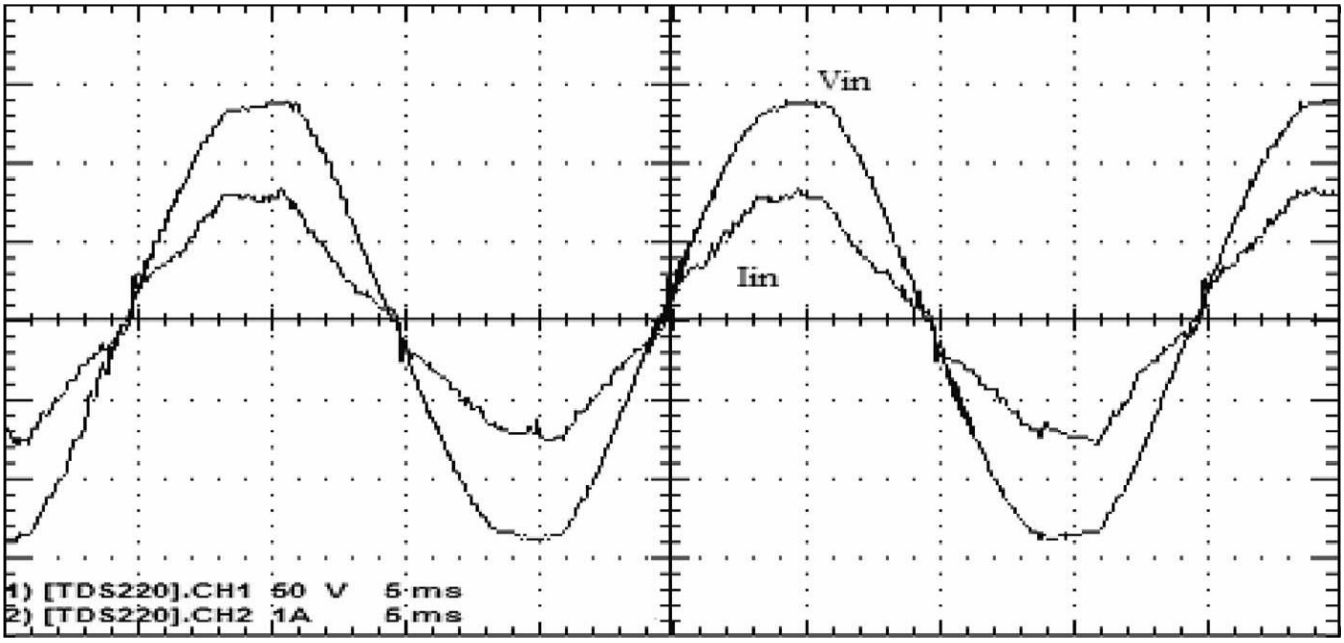


Fig 5: Measured input voltage and filtered input current at full load (THD =8.2%)

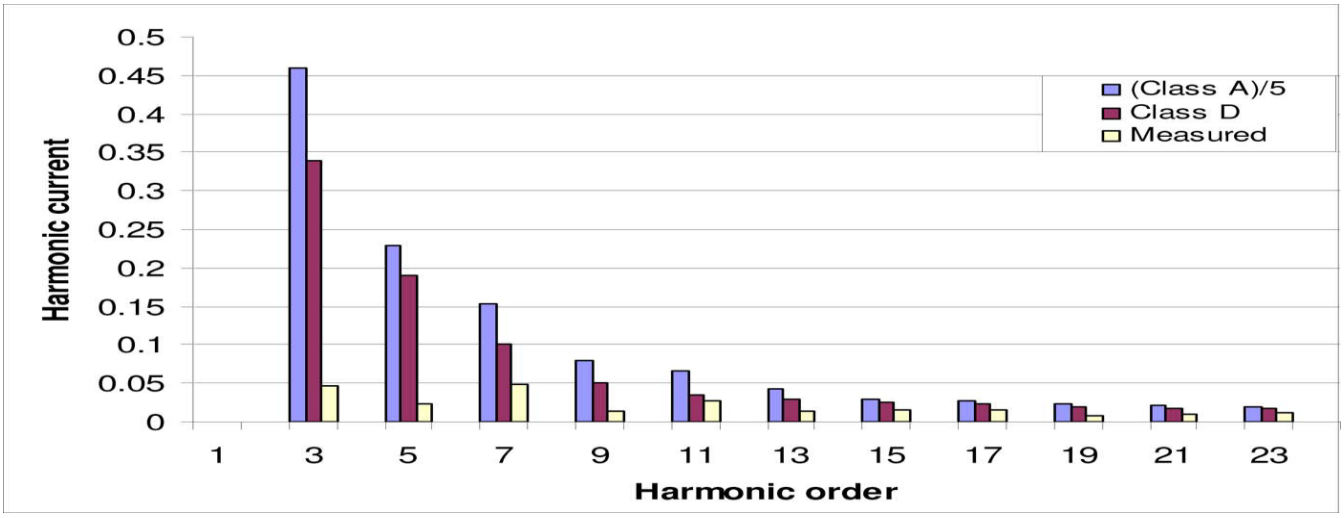


Fig 6: Measured harmonics content of the input current

III. SIMULATION RESULTS

In order to verify the proposed concept, a prototype of the converter shown in Fig. 2 was constructed and experimentally tested. To ensure proper operation of the converter, the dc bus voltage (*VCB*) must be higher than the input voltage, such that the diode *D*1 is OFF and the inductor *LB* stores energy when the switch (SW) is ON. Therefore, from (15) the inductor *Lm* must be higher than the input inductor *LB*. The DCM flyback converter was designed and implemented for 50 V/80 W output, *V*in,rms (100–240 V) universal line voltage, and overall efficiency of 86% is assumed. The switching frequency is selected to be 100 kHz and the maximum duty cycle of is 0.45. The major components of the circuit are follows: transformer turns ratio (*N*1 = 30,*N*2 = 10,*N*3 = 15) with core ETD34, *Lm* = 200 μH, *LB* = 80 μH, *CB* = 47 μF, *Ca* = 22 μF, *Co* = 470 μF, the switch SW (SPW22N60), the bridge rectifier and diodes *D*1,*Do* using MUR1560.

Fig. 5 shows the measured input voltage and filtered input current waveforms for a 100 Vac input voltage at full load. As it may be seen from Figs. 4 and 5, that selecting the turns ratio *N*3/*N*1 and the dc bus voltage *VCB* can be optimized in order to reduce the dead time and improve the quality of the input current. Fig. 6 shows the

measured harmonic content of the input current compared to the Classes A and D regulation standards. Note that, in order to improve the visibility of the higher order harmonics, class A limits are scaled down by a factor of 5 (class A limits/5). The measured THD = 7% and the power factor is 0.997. Obviously, the input current is much closer to the sinusoidal waveform and it meets the regulation standards. Fig. 7 shows the transient response of the converter for a step change of load between 50% and 100%. It may be seen that a fast dynamic response has been obtained.

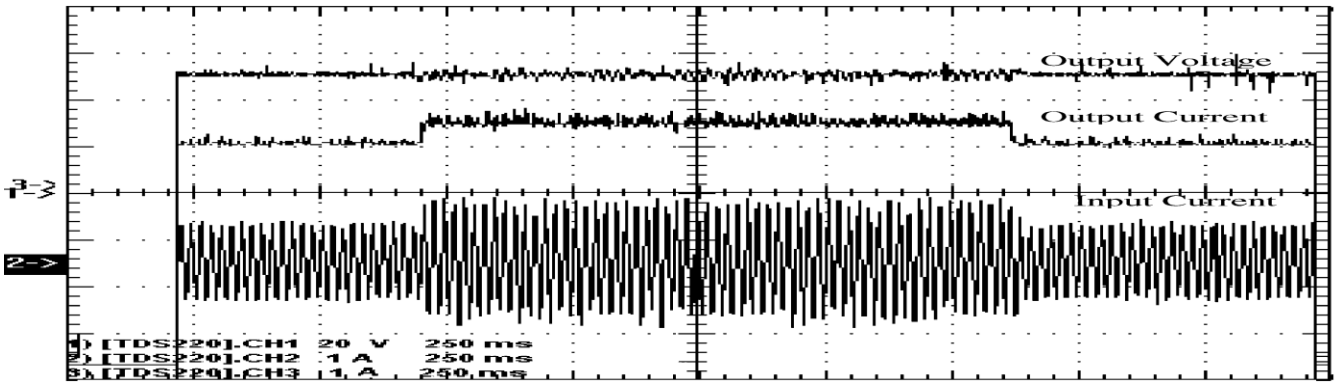


Fig. 7. Response between 50% and 100% of load. (Top–bottom): output voltage (CH1), output current (CH3), input current (CH2).

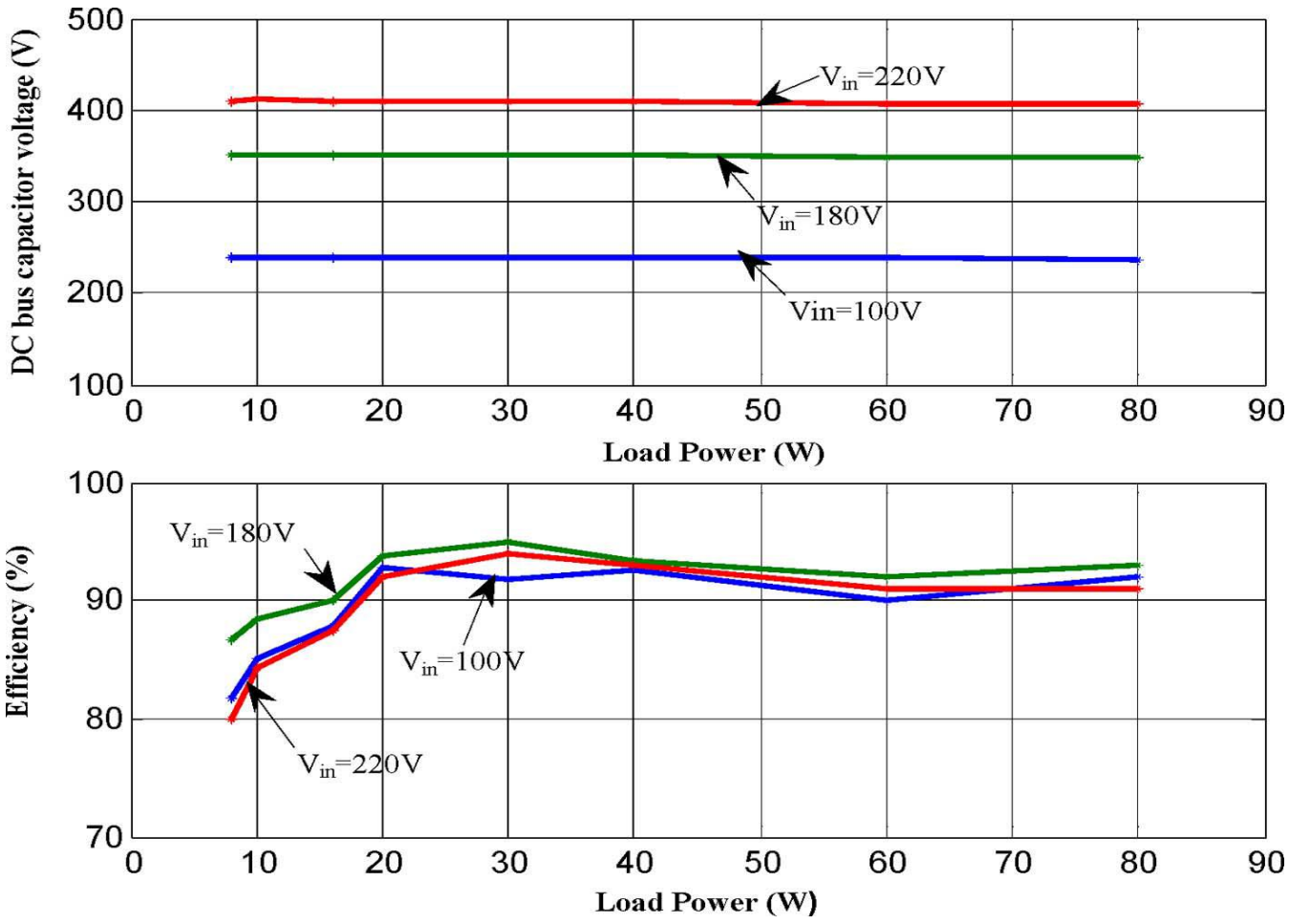


Fig. 8. Measured dc bus capacitor voltage and efficiency versus load power for a range of input voltage.

TABLE I:COMPARISON BETWEEN THE CONVENTIONAL BOOST + FLYBACK AND THE ROPOSED PFC CIRCUIT

	Boost+flyback (DCM+DCM)	Proposed converter(DCM+DCM)
Semiconductors	3 diodes, 1 switch, 1 bridge rectifier	2 diodes, 1 switch, 1 bridge rectifier
Passive components	1 inductor, 2 capacitors, 2-winding Transformer	1 inductor, 3 capacitors, 3-winding Transformer
Switch current	$I_{LB}+I_{Lm}$	$(N_3/N_1)I_{LB}+I_{Lm}$, where $N_3/N_1<1$
Efficiency (at full load)	70%	>90%
Capacitor voltage V_{CB} (for constant input voltage)	Controlled by the ratio L_m/L_B	Controlled by the ratio L_m/L_B and winding ratio N_3/N_1
THD of the input current	>20%	<10%

Fig. 8 shows the measured dc bus voltage *VCB* and efficiency of the converter for range of load and input voltage variation. It may be seen that the capacitor voltage can be maintained below 450 V by properly designing the turns ratio *N*3/*N*1 and the inductors ratio *Lm/LB*. Furthermore, the proposed converter can maintains 90% efficiency or above at high load. Finally, Table I summarizes the comparison between conventional single-stage boost-flyback converters [1], [2] and the proposed converter in terms of circuit construction and performance. It may be seen, that the proposed converter presents a high quality input current with THD <10% and high efficiency. However, the proposed converter has additional winding *N*3 in series with capacitor (*Ca)*, but they are small in size since *N*3 operate at the converter switching frequency.

IV. CONCLUSION

In this letter, a new ac/dc converter based on a quasi-active
PFC scheme has been presented. The proposed method produces a current with low harmonic content to meet the standard specifications as well as high efficiency. This circuit is based on adding an auxiliary winding to the transformer of a cascade dc/dc DCM flyback converter. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a tradeoff between efficiency and harmonic content can be established to obtain compliance with the regulation and efficiency as high as possible. Operating principles, analysis, and simulation results of the proposed method are presented.

REFERENCES

[1] O. Gracia, J. A. Cobos, R. Prieto, and J. Uceda, "Single-phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.

[2] R. Redle, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power factor correctors with fast regulation of the output voltage," in *Proc. IEEE PESC 1994 Conf.*, pp. 1137–1144.

[3] C. Qian and K. Smedley, "A topology survey of single-stage power factor with a boost type input-current-shaper," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 360–368, May 2001.

[4] T.-F. Wu, T.-H. Yu, and Y.-C. Liu, "An alternative approach to synthesizing single-stage converters with power factor correction feature," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 734–748, Aug. 1999.

[5] L. Huber, J. Zhang, M. Jovanovic, and F.C. Lee, "Generalized topologies of single-stage input-current-shaping circuits," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 508–513, Jul. 2001.

[6] H. Wei, I. Batarseh, G. Zhu, and K. Peter, "A single-switch AC-DC converter with power factor correction," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 421–430, May 2000.

[7] L. K. Chang and H. F. Liu, "A novel forward AC/DC converter with input current shaping and fast output voltage regulation via reset winding," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 125–131, Feb. 2005.

[8] H. L. Do, "Single-stage single-switch power factor correction AC/DC converter," *Inst. Electr. Eng. Proc. Electr. Power Appl.*, vol. 152, no. 6, pp. 1578–1584, Nov. 2005.

[9] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch power factor correction ac/dc converters with dc-bus voltage feedback for universal line applications," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1079–1088, Nov. 1998.

[10] S. Luo,W. Qiu,W.Wu, and I. Batarseh, "Flyboost power factor correction cell and a new family of single-stage AC/DC converters," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 24–33, Jan. 2005.

[11] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifiers-regulators by variablefrequency control," in *Proc. IEEE APEC 1994 Conf.*, pp. 569– 575.

[12] J. Sebastian, A. Femandez, P. Villegas, M. Hemando, and J. Prieto, "New topologies of active input current shapers to allow AC-to-DC converters with asymmetrically driven transformers to comply with the IEC-1000-3-2," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 493–501, Jul. 2002.

[13] N. Vazquez, J. Lopez, J. Arau, C. Hernandez, and Elias Rodriguez, "A different approach to implement an active input current shaper," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 132–138, Feb. 2005

[14] K. Zhou, J. G. Zhang, S. Yuvarajan, and D. F. Weng, "Quasiactive power factor correction circuit for switching power supply," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1410–1414, May 2008.