DESIGN OF FPEZ-SOURCE NETWORK WITH REDUCED SWITCHES FED INDUCTION MOTOR

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ABSTRACT
This Project deals with an fully parallel Embedded Z-source inverter(FPEZ) to control the three phase induction motor. Z-Source inverter is a single-stage converter which performs both buck-boost energy conversions using the LC impedance network. The further advancement in the Z-Source inverter is the partially parallel Embedded Z-Source(PPEZS) inverter that can produce same gain as Z-Source inverter but with lower capacitor voltage and ripples . In order to overcome the drawbacks of PPEZS, Fully parallel EZ-(FPEZS) Source inverter is proposed. The proposed inverters provide a high boost voltage inversion ability, a lower voltage stress across the active switching devices and capacitors with a continuous input current. In addition, they can suppress the startup inrush current, which otherwise might destroy the devices. The proposed system reduces six switch three phase inverter to four switch three phase inverter. This makes system compact which reduces cost and switching losses, line harmonics, improves power factor, reliability and extends the output voltage range. The system is modeled using Proteus and Simulink simulation. This paper presents the operating principles, analysis, and simulation results of FPEZ Source inverter.

KEYWORD
Boost inversion ability, Buck-boost ,Embedded Z source, Motor drives, PEZS, PWM, voltage boost, Z Source Inverter.

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1. INTRODUCTION

Inverters are the dc to ac converters. The input dc supply is either in the form of voltage or current is converted in to variable output ac voltage. The output ac voltage can be controlled by varying input dc supply or by varying the gain of the inverter. There exists two traditional converters, voltage-source and current-source converters, either rectifier or inverter depending on power flow directions. There are some limitations in those two inverters.

1.1 Voltage source inverter (VSI)

VSI is a 3-Ø bridge inverter fed from DC voltage source (or) AC voltage source with diode rectifier and antiparallel diode to provide bidirectional current flow and unidirectional voltage blocking capability as shown in fig 1.1.

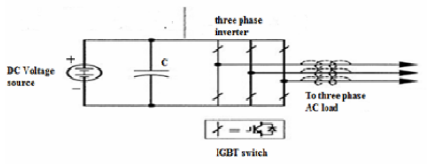

Fig 1.1:Voltage Source Inverter

1.2 . Current source inverter (CSI)

CSI is 3-Ø bridge inverter fed from current source(i.e) a voltage source in series with large inductor and series diode to provide unidirectional current flow and bidirectional voltage blocking as shown in fig 1.2.

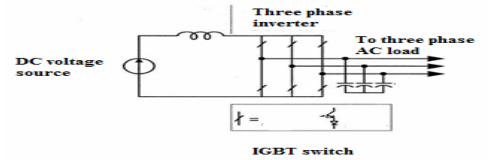

Fig 1.2: Current Source Inverter.

In addition, both the V-source converter and the I-source converter have the following common problems.

• They are either a boost or a buck converter and cannot be a buck–boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage.

• They are vulnerable to EMI noise in terms of reliability.

A Z-source inverter could elevate most of the problems associated with traditional voltage source and current source inverters. Unique features of the Z-source inverter provide a cheaper, simpler, and single stage power conversion structure for induction motor drives. Presence of Z-network highly enhances the reliability of the inverter since the shoot-through can no longer destroy the inverter.

II. IMPEDANCE SOURCE

2.1.Impedance Source Network:

Impedance networks provide an efficient means of power conversion between source and load in a wide range of electric power conversion applications (dc-dc, dc-ac, ac-dc, ac-ac). Z-Source is the X –Shaped structure consists of L1, L2, C1, C2 in which we can obtain both buck-boost operations in

single stage conversion.Various topologies and control methods using different impedance source networks have been presented, *e.g.* for adjustable-speed drives (ADS), uninterruptible power supply (UPS), distributed generation (fuel cell, PV, wind, *etc.*),battery or super-capacitor energy storage, electric vehicle, distributed dc power systems, avionics,flywheel energy storage systems, electronic loads, dc circuit breaker and etc. Fig 3 shows the power circuit configuration of the Z-source inverter fed induction motor drive system.

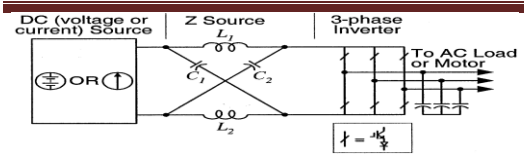

Fig. 2.1. Z-source converter structure using the series combination of switching device and diode.

2.2.Equivalent Circuit &Modes Of Operation**:**

The DC source/load can be either a voltage or a current source/load. The unique feature of the Z-source inverter is that the output ac voltage can be any value between zero and infinity regardless of the input DC voltage. That is, the Z-source inverter is a buck–boost inverter that has a wide range of obtainable voltage. The three-phase Z-source inverter bridge has nine permissible switching states unlike the traditional three-phase V-source inverter that has eight.The traditional three-phase V-source inverter has six active vectors when the DC voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices,respectively. However, three-phase Z-source inverter bridge has one extra zero state (or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on),any two phase legs, or all three phase legs

Mode I:

In this mode, the inverter bridge is operating in one of the six traditional active vectors; the equivalent circuit is as shown in figure 4.

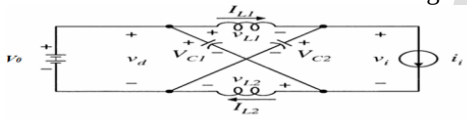

Fig.2.2: Equivalent Circuit of the ZSI in one of the Six Active States

The inverter bridge acts as a current source viewed from the DC link.

Mode II:

The equivalent circuit of the bridge in this mode is as shown in the fig. 5

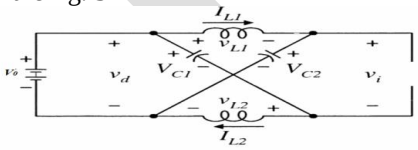

Fig. 2.3: Equivalent Circuit of the ZSI in one of the Two Traditional Zero States

The inverter bridge is operating in one of the two traditional zero vectors and shorting through either the upper or lower three device, thus acting as an open circuit viewed from the Z-source circuit.

Mode III:

The inverter bridge is operating in one of the seven shoot-through states.The equivalent circuit of the inverter bridge in this mode is as shown in the fig 6. `

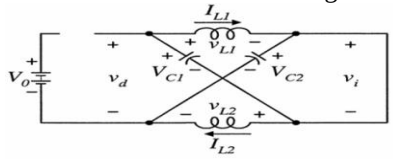

Fig.2.4: Equivalent Circuit of the ZSI in the Shoot-Through State.

In this mode, separating the dc link from the ac line. This shoot-through mode to be used in every switching cycle during the traditional zero vector period generated by the PWM control.

***Shoot-Through*(Sx= Sx_ON, x = A, B, or C; D = OFF)**

$V_L=V_C$, $V_i=0$, $V_d=2V_C$ (2.1)

$V_D=V_{dc}-2V_C$ (2.2)

$I_L=-I_C$, $I_i=I_L-I_CI_{dc}=0$. (2.3)

Non-shoot-Through (Sx≠Sx_, x = A, B, or C; D = ON)

$V_L=V_{dc}-V_C$ (2.4)

$V_i=2V_C-V_{dc}$, $V_d=V_{dc}$ (2.5)

$I_{dc}=I_L+I_C$,$I_i=I_L-I_CI_{dc}\neq 0$. (2.6)

In this DC Source is placed at far-left in series with diode. So, by this, chopping is occurred in the source current which is caused by the commutation of diode D . So, in this condition to smoothen the source current an additional LC filter is required which would rise over all cost of the system and construction of the system by this additional LC filter is complex.

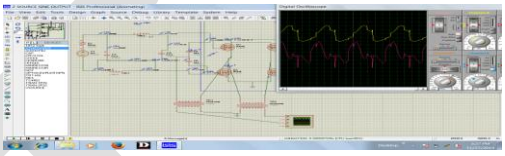

Fig2.5; Chopping ripples source current in Z source

So, to overcome the above drawbacks, a new technique is proposed i.e.Embedded source inverter. In this EZ-Source inverter, source is placed in series with the inductor L1 and L 2 and chopping current (i.e.) Obtained in the previous section is filtered. EZ-Source inverter, smoothens the source current without any additional LC filter but the gain of the Z-Source and EZ-Source is same but only source filtering is achieved without any additional LC filter.

III. EMBEDDED Z SOURCE INVERTER

Parallel embedded Z-Source inverters:

Besides the shunt embedded Z-Source inverters,an alternative topology with dc sources inserted into the X shaped network is the parallel embedded Z-Source inverter .In this we have fully parallel embedded Z-Source inverter and partially parallel

Inverter

Types Of Parallel EZ Source:

1.Partially Parallel Embedded Z Source-(PPEZ)

2.Fully Parallel Embedded Z Source(FPEZ)

3.1.Partially parallel embedded Z (PPEZ)-Source inverter:

In this a single DC source is connected to one of the inductor in the series, due to this unequal voltage distribution exists b/w capacitor C1& C2 and a symmetric distribution to electrical stem still remain lower voltage and stress across the capacitor while comparing with traditional network.

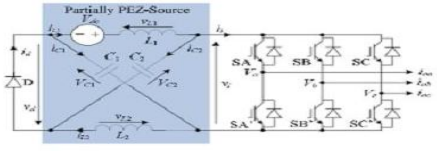

Fig3.1:PartiallyParallel Embedded Z Source.

Non shoot-through state(Sx≠Sx_, x = A, B, or C; D = ON)

$V_{L1}=Vdc-vc2$ ----------(3.1)

$Vi=vc1+vc2$ ----------(3.2)

Shoot through state(Sx= Sx_ON, x = A, B, or C; D = OFF)

$V_{L1}=Vdc+vc1$ ----------(3.4)

$Vi=0$ -- ---------(3.5)

3.2.Fully parallel EZ Source(FPEZ):

In this two dc sources are parallel in which it is placed in series with an inductor. So by these chopping currents of source due to commutating of diode D is reduced and pure DC is produced and that is given to 3-ø inverter. In this diode itself acts as the switch and control the unnecessary condition that are occurred due to inverter. In this the voltage stress across the capacitor is equal due to placing of two DC sources and having
increased AC output voltage.

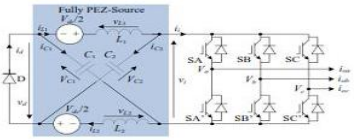

Fig 8.Fully Parallel EZ Source

shoot-Through(Sx= Sx_ON, x = A, B, or C; D = OFF)

$V_L = V_C + V_{dc}/2$ (3.5)

$V_i = 0$ (3.6)

$V_d = V_D = -2V_C$. (3.7)

$I_L = -I_C$, $I_i = I_L - I_C$ (3.8)

$I_{dc} = 0$. (3.9)

Non-shoot-Through (Sx≠Sx_, x = A, B, or C; D = ON)

$V_L = V_{dc}/2 - V_C$ (3.10)

$V_i = 2V_C$ (3.11)

$V_d = V_D = 0$ (3.12)

$I_{dc} = I_L + I_C$, $I_i = I_L - I_C$ (3.13)

$V_P = V_{dc}/(1-2D)$. (3.14)

$V_{ac} = MV_P/2$. (3.15)

IV.IMPLEMENTATION OF FPEZ FED INDUCTION MOTOR

4.1.System Overview:

Block diagram of the FPEZ-Source inverter fed induction motor drive system is shown in the fig.4.1

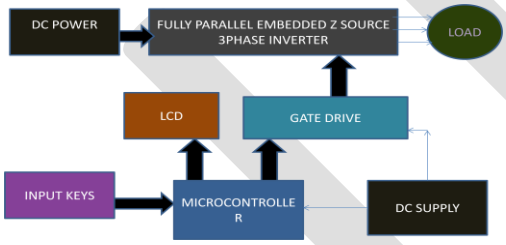

Fig 4.1

Block Diagram of FPEZ

DC voltage source can be a battery, fuel-cell stack, diode rectifier, and/or capacitor. An impedance network abbreviated as FPEZ-Source is couples the inverter main circuit and input power source. FPEZ-Source circuit consists of Two sources, two capacitors and two inductors connected in such a way as to form second order filter, smoothens dc link voltage and current. Three phase inverter circuit consists of Four switches connected in three legs, converts input dc link voltage in to corresponding three phase ac voltage.

Microcontroller and driver circuit is used to control on/off time of switching devices in a proper sequence in a particular time used in the main inverter circuit. Microcontroller used to generate modified maximum constant boost PWM signal. These PWM signal is applied to the gate terminals of MOSFETs/IGBT through gate driver circuit.

4.2. Control Circuit:

Modified maximum constant boost PWM control method is most advantageous over the other PWM control methods. In this method shoot-through duty ratio and hence boost factor is maintained constant form cycle to cycle. It also reduces voltage stress across switching devices and improves performance .

PWM switching pattern

State	C'	B'	A'	C	B	A	PWM code(hex)
S1	1	0	1	0	1	0	0x2a
S2	1	0	0	0	1	1	0x23
S3	0	0	1	1	1	0	0x0e
S4	0	1	1	1	0	0	0x1c
S5	0	1	0	1	0	1	0x15
S6	1	1	0	0	0	1	0x31
Zero1	1	1	1	0	0	0	0x38
Zero2	0	0	0	1	1	1	0x07
ST	0	0	0	0	0	0	0x00

Table1:PWM Switching pattern generation

PWM switching pattern

Table 1 shows all possible PWM states for Z-source inverter and respective PWM code pattern. The letters A, B, C indicates upper three switching devices and A‟, B‟, C‟ indicates lower three switching devices in three arms of the main inverter circuit.

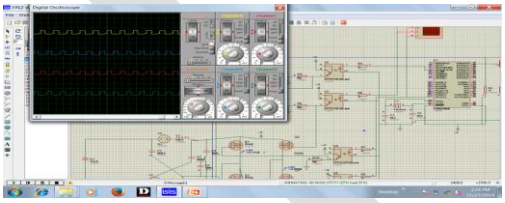

Fig4.2:PWM waveform of Proteus simulation

As shown in table PWM for Z-source inverter consists of six active states s1-s6, two zero states and a shoot-through state (ST).

V. DESIGN OF FPEZ WITH REDUCED SWITCHES FED IM MOTOR:

In generally, by using six switches in three phase inverter produces losses of the six switches and also Increases the complexity of the control algorithms. So to overcome that 4-switch three phase(4S3P) inverter is proposed,

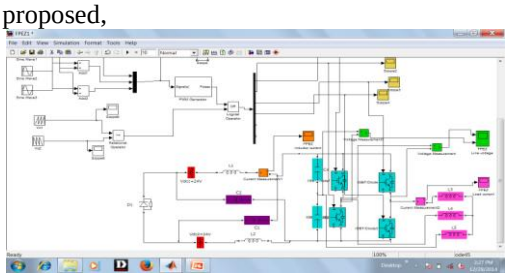

Fig:5.1 FPEZ with 4S3P

Fig:5.2 Capacitor voltage of FPEZ Source

Line voltage

Line voltage(VL)=√3*Vph

=√3*49.6=86.42V(theoretical)

FPEZ =VL1= 80-85V(practical)

VL2=80-83V(practical)

Phase voltage

Phase voltage (Vp)=M*B*Vdc/2

Modulation index=0.8,

Boost factor=2.604,Vdc=48

=(0.8*2.604*48/2)=49.6(Theoretical)

=47.7(Practical)

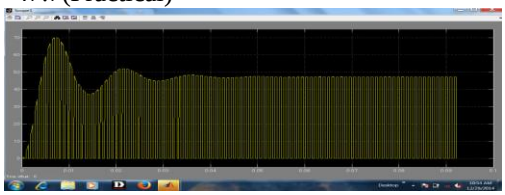

Fig 5.3: Phase voltage of simulink FPEZ

PPEZ	FPEZ
Vdc=48V	Vdc=48V
Vc=72V(T) Vc=60V(p)	Vc=72V(T) Vc=70.1V(P)
Vp=49.6V(T) Vp=46.8V(P)	Vp=49.6V(T) Vp=47.3V (P)
Vline=86.4V(T) Vline=50-80V(P)	Vline=86.4V(T) Vline=80-85V(P)

So by this FPEZ-Source inverter with reduced switches reduces switching losses and number of interface circuits to supply logic signals for the switches reduce,s price due to reduction in number of switches and less chance of destroying the switches due to lesser interaction among switches and less real-time computational burden.

VI.SIMULATION & HARDWARE RESULTS

The fully parallel embedded Z-Source inverter with reduced switches converts filtered, ripple free pure DC into three phases AC. Three phase balanced AC thus obtained through fully parallel embedded Z-Source inverter with reduced switches is fed to an asynchronous machine like induction motor for its effective control.

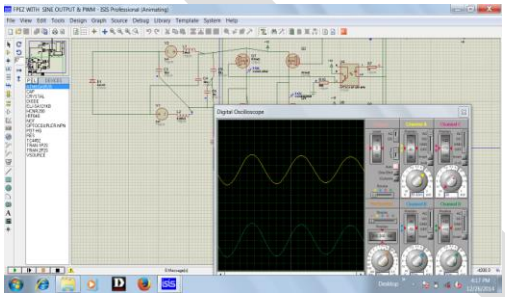

Fig:6.1 Simulation of FPEZ(4s3p) using Proteus

FPEZ-Source inverter with reduced switches fed IM drives is simulated using Proteus and ulink simulation results are obtained given below.

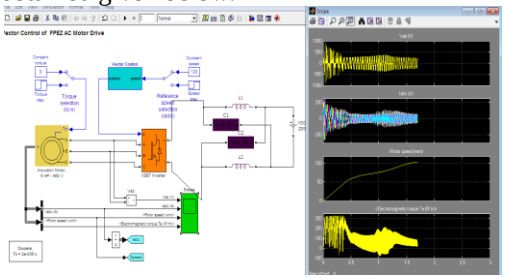

Fig6.2 : FPEZ with (4S3P)inverter Using Simulink with its torque,frequency,speed characteristics

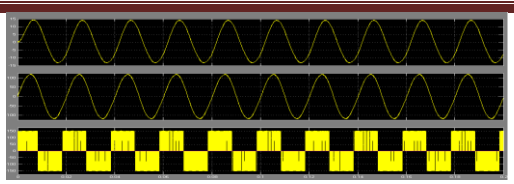

Fig6.3 :line current and line voltage of FPEZ Source inverter.

VII. CONCLUSION:

This paper has proposed a new family of Embedded Z-source inverters implemented using an impedance network with the relevant dc sources embedded within.

Results of simulation are compared with traditional PWM inverter in Table

Table:7.1Comparison Table of Embedded Z Source

Following results are observed,

1. Shoot-through state is allowed by switching on all devices in the main inverter, thus EMI noise does not affect operation of FPEZ-source inverter.

2. The low frequency ripples in the inductor current and capacitor voltage are eliminated completely.

3. Output voltage can be boosted to any desired value by varying shoot-through period T0, in zero states without changing active state for a fixed modulation index.

4. Component size (L & C) and hence cost required is less as compared to traditional PWM inverter .

The Fully parallel embedded Z-Source inverter with reduced switches reduces Capacitor rating, smoothens source current and also reduce total harmonic distortion.

REFERENCES:

[1] S.Kamalakkannan, S.Deve Gowda, “Digital simulation of renewable Energy Source Controlled EZ-Source inverter system”, 2012 IEEE.

[2] Ding Li, Poh Chiang Loh, Miao Zhu, Feng GAO, Frede Blaabjerg,”Multi-cell Trans-Z-Source Inverter”, IEEE PEDS 2011, Singapore, 5-8 Dec.2011

[3] Nisha K.C.R, T.N.Basavaraj,” Closed loop Controlled Solar Cell Powered Embedded EZ-Source Inverter Fed Induction

Motor Drives”, ACEEE Int.J.on Control system andInstrumentation, Vol.4, No.2, June , 2013.

[4] K.Srinivasan and Dr.S.S.Dash, “Performance Analysis of a

Reduced Switch Z-Source Inverter Fed IM Drives”,International Journal of Computer and Electrical Engineering, Vol.2, No.4, August.2010.

[5] F.GAo, P.C.Loh, F.Blaabjerg and C.J.Ganjanayake, “Operational Analysis and Comparative Evaluation of Embedded Z-Source Inverter”, IEEE 2008.

[6] F.Z.Peng, “Z-Source inverter”, IEEE Trans.Ind.Appl.,vol.39, no.2,pp.504-510,Mar/Apr.2003.