Design Diagnosis and Fault-Tolerant Control of Three-Phase AC–DC PWM Converter Systems Of Testing Process

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***Abstract*—There is the possibility of an open-switch fault in a three-phase ac–dc pulsewidth-modulation (PWM) converter due to problems with the switching devices. In this case, the converter causes unbalanced input ac currents including increased harmon-ics and dc-link voltage ripples. In this paper, the one-open-switch fault case of six switching elements is analyzed by considering the switching patterns of space vector PWM and the directions of a faulty phase current to prove the cases of the fault. In addition, this paper proposes a detection method for open-switch faults and a fault-tolerant control method to minimize the imbalance of the input ac currents and the voltage ripple of the dc link in a three-phase ac–dc PWM converter. The usefulness of this paper is verified through experimental results.**

***Index Terms*—Active rectifier, diagnosis, fault detection, fault-tolerant control, pulse width-modulation (PWM) converter.**

I. INTRODUCTION

THREE-PHASE pulse width-modulation (PWM) ac–dc co-nverters have been increasingly employed in recent years owing to their advanced features including a sinusoidal input current with a unity power factor and a controllable high-quality dc output voltage [1]. It is estimated that about 38% of the faults in power conversion systems are due to failures in power de-vices such as insulated-gate bipolar transistors (IGBTs). IGBT failures can be broadly categorized into open-switch faults, short-circuit faults, and intermittent gate-misfiring faults [2]. If a short-circuit fault occurs in the voltage-source conversion system, it will cause a system shutdown. Hence, its source is blocked by protection circuits such as circuit breakers or fuses. Otherwise, the system will be destroyed due to switching and peripheral device damages. On the other hand, an open-switch fault does not cause a system shutdown but degrades the system performance. In this case, the converter causes unbalanced input ac currents including harmonics and a ripple in the dc-link voltage. These may, in turn, cause secondary faults. If such abnormal operation continues for a period of time, the accu-mulated fatigue under unstable operation may result in mal-functions of the PWM converter. Accordingly, there is high possibility of secondary faults in the converter system, the load, and the grid. Therefore, a diagnostic technique for the PWM converter is required for the monitoring and detection of open-switch faults.

If faults occur in the converter system, an emergency stop should be executed, and some maintenance should be per-formed. However, an emergency stop cannot be made available in special applications such as semiconductor or steel manufac-turing processes. Therefore, both diagnostic methods and fault-tolerant control methods are required [3]–[6].

Many diagnosis and fault tolerance control methods for a dc–ac inverter have been developed during the last decade [7]–[11]. However, there are a few research works for an ac–dc converter. The inverter and the converter have different current patterns under the same condition of IGBT open-switch fault. Accordingly, it is difficult to apply the same kind of diagnostic methods used for the inverter to the converter. A diagnosis method used the derivative of the current vector's angle and the mean values of phase currents for fault alarm and fault localization, respectively [12]. On the other hand, many fault tolerance control methods for the inverter can be applied to the converter, but they require additional circuits for redundancy.

This paper proposes a diagnostic method for open-switch faults and a fault-tolerant control method in three-phase ac–dc PWM converters. The open-switch fault of a converter is detected by using the derivative of the current vector's angle, and the faulty switch can be found from the

phase angle. Then, the fault-tolerant control can be applied by simply revising the PWM switching pattern. This tolerance control can improve the efficiency and power factor of the PWM converter by reducing the current imbalance and the harmonics of the ac grid current. In addition, the ripple of the dc-link voltage can be reduced considerably. Therefore, the reliability of the converter system utilizing the proposed methods is significantly increased due to the performance improvement and the secondary fault probabil-ity reduction. The attractive feature of the proposed methods is that they are easily implemented by simply changing the PWM switching pattern without adding any external hardware (H/W) circuits. The usefulness of this paper is verified through the experimental results.

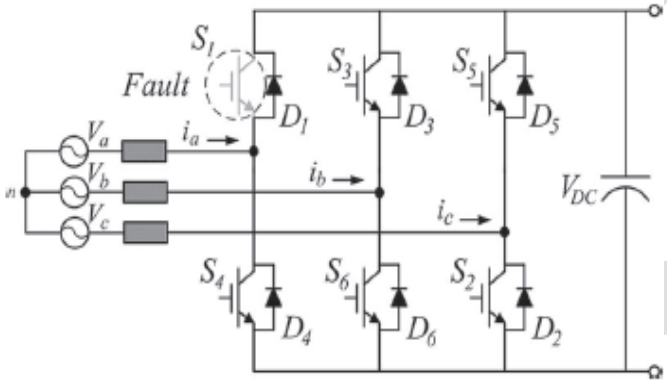

Fig. 1. Three-phase ac–dc converter with an open-switch fault in S_1 (the top switch of the *a* phase).

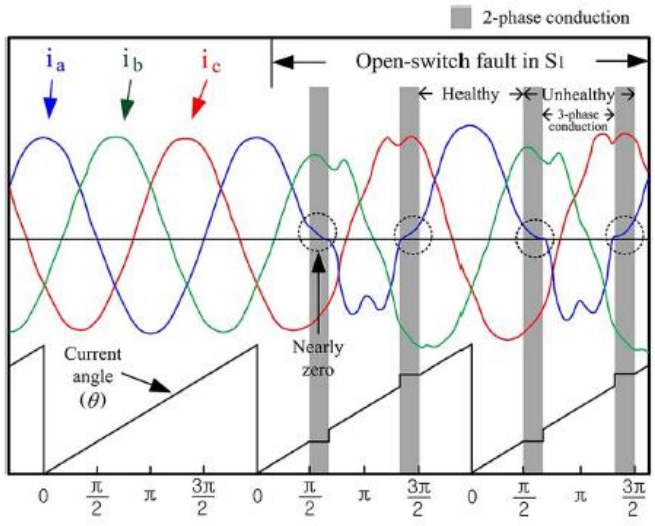

Fig. 2. Three phase currents and current angle before and after the open-switch fault in S_1.

II. DIAGNOSIS OF OPEN-SWITCH FAULTS

Three-phase ac–dc PWM converters provide a controllable dc-link voltage and a unity power factor by using high-performance controllers including both space vector PWM (SVPWM) and synchronous current regulators. Converters with an open-switch failure have different current patterns when compared with three-phase voltage-source inverters (VSIs) with an open-switch fault. This is because most of the currents in an ac–dc converter mainly use freewheeling diodes except in several operation regions [13]–[16]. Hence, even when there is an open-switch fault in one of the six switches in a PWM converter, either the positive or negative current is not perfectly blocked as is the case with a VSI fault. Converter faults have various current shapes depending on the dc-link voltage, the load, and the control conditions of the converter [17].

For example, if an open-switch fault occurs on the top switch of the *a* phase, as shown in Fig. 1, the input ac currents are distorted, as shown in Fig. 2. The *a*-phase current is not affected during the positive half cycle but is distorted during the negative half cycle because the positive current of the *a* phase flows through diode D_1 or switch S_4 and the negative current of that flows only through diode D_4 excluding switch S_1. As shown in Fig. 2, the faulty phase current remains nearly zero in the shaded narrow bands because the phase current cannot flow through S_1 as mentioned earlier. Then, the converter acts as a single-phase conduction operation instead of a three-phase conduction operation. Hence, an open-switch fault can be de-tected by using this phenomenon [18].

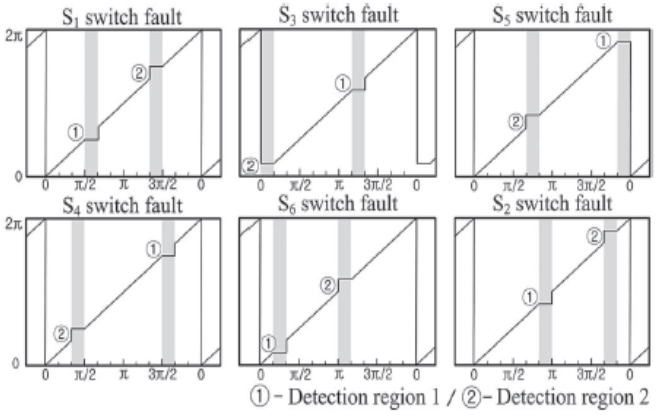

Fig. 3.Current angles of six cases with every one-open-switch fault.

Three-phase input ac currents can be represented as follows in the two-phase stationary reference frame [19], [20]:

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$$i_d^s = \frac{2}{3} i_a - \frac{1}{3}(i_b + i_c)$$
$$i_q^s = \frac{1}{\sqrt{3}}(i_b - i_c) \qquad (1)$$

where i_a, i_b, and i_c are the three phase input currents and i^s_d and i^s_q are the two phase currents of the stationary reference frame. The magnitude and the current angle of (1) are given in the following:

$$\left|i_{dq}^s\right| = \sqrt{i_d^{s^2} + i_q^{s^2}}$$
$$\theta = \begin{cases} \tan^{-1}\left(i_q^s / i_d^s\right), & i_d^s \geq 0 \\ \tan^{-1}\left(i_q^s / i_d^s\right) + \pi, & i_d^s < 0. \end{cases} \qquad (2)$$

In the steady state, the magnitude of the current vector is constant, and the current angle rotates constantly with the grid frequency. The derivative of the current vector's angle θ during one sampling period can be derived by the following:

$$\Delta\theta = \omega T_S = \tan^{-1}\left(\frac{i_d^s[n]}{i_q^s[n]}\right) - \tan^{-1}\left(\frac{i_q^s[n-1]}{i_d^s[n-1]}\right) \qquad (3)$$

where ω is the grid frequency and T_S is the sampling period of the current regulator. Without an open-switch fault, θ is ideally constant. However, in case of an open-switch fault, θ remains around zero during the shaded narrow bands, as shown in Fig. 2. This means that the rotating current vector is stopped during those shaded bands.

Fig. 3 shows the current angles of six cases with a one-open-switch fault. Table I shows the fault detection regions in Fig. 3. Detection region 1 is the starting region of the current distortion, and detection region 2 is an ending region of the current distortion. The angle difference is $2\pi/3$ between the two regions.

Fig. 4 shows the flowchart of the proposed diagnosis method for open-switch fault detection. The threshold value of the flowchart can be represented by the following:

$$\text{th} = K \times \omega T_S = K \times \theta \qquad (4)$$

where K is a constant between zero and one. If the value of K is too high, the comparator in Fig. 4 is sensitive to current switching noise. On the other hand, if the value of K is too low, fault detection may not work. Thus, 0.5 has been chosen to be the most suitable value by experimental experience. If a fault occurs, θ becomes lower than the threshold value because the variation is decreased by the fault, as shown in Fig. 2. If the first condition is satisfied in the second line in Fig. 4, the fault detection loop is activated. Then, the faulty switching element is loaded from Table I to the fault detection algorithm to verify the selected switching element. If the variation in the fault angle stays below the threshold value during T_{fault}, it is determined that the selected switching element has failed.

TABLE I

FAULT DETECTION REGIONS DEPEND ON THE FAULT OF EACH OPEN SWITCH

Fault switch	Detection region 1	Detection region 2
S_1	$\pi/2 \sim 2\pi/3$	$4\pi/3 \sim 3\pi/2$
S_2	$5\pi/6 \sim \pi$	$5\pi/3 \sim 11\pi/6$
S_3	$7\pi/6 \sim 4\pi/3$	$0 \sim \pi/6$
S_4	$3\pi/2 \sim 5\pi/3$	$\pi/3 \sim \pi/2$
S_5	$11\pi/6 \sim 0$	$2\pi/3 \sim 5\pi/6$
S_6	$\pi/6 \sim \pi/3$	$\pi \sim 7\pi/6$

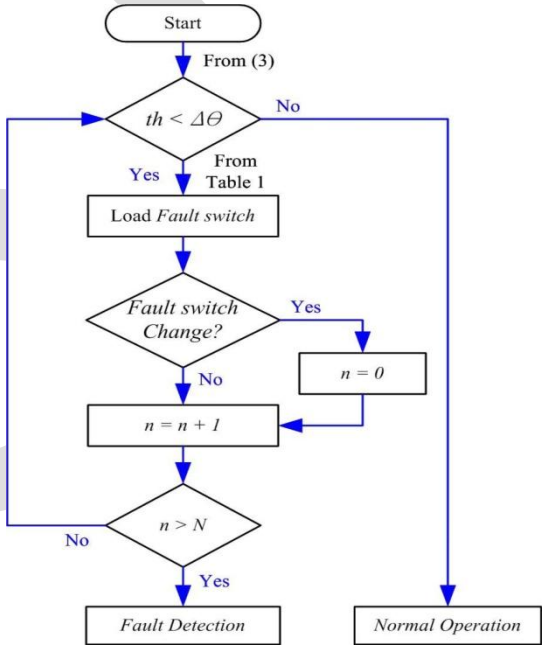

Fig. 4. Proposed flowchart of the open-switch fault detection.

Otherwise, the detection algorithm iterates until it detects the faulty switching element. If the fault detection time is too long, the detection range exceeds the shaded narrow bands in Fig. 2. This means that detection of the fault is impossible. If the fault detection time is too short, there is the possibility of a false detection due to switching noise and sensing error. The fault detection time can be given as in the following:

$$T_{\text{fault}} = N\,T_S \qquad (5)$$

where N is the comparison number of the detection algorithm and is directly related to the sampling time of the current regu-lator and the grid frequency. For example, if the grid frequency is 60 Hz and the sampling time (T_S) is 100 μs, 13 times can be sampled during one detection region of $\pi/6$. In this paper, the most suitable number has been shown to be eight according to experimental experience. When the counter value (n) of the flowchart is more than 8 among 13 in one detection region, the fault can be detected. Therefore, this method is robust to intermittent interference and noise less than 800 μs.

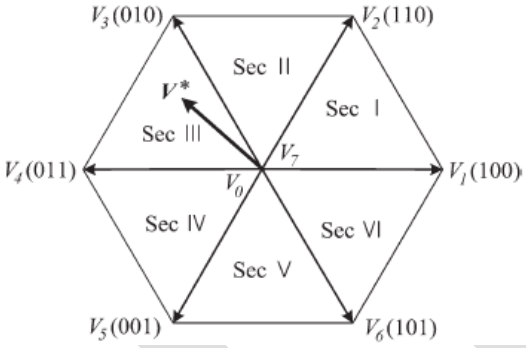

Fig. 5. Reference voltage V^* in Sec III of the hexagon of SVPWM.

This diagnosis method uses only the phase angle of the cur-rent vector which is rotated with the grid frequency. Therefore, despite the sudden load variations, it can prevent the misinter-pretation of transients because the magnitude is irrelevant [18].

On the other hand, when the voltage supply from the power grid is seriously unbalanced or distorted by unwanted harmon-ics, false alarms for the fault detection can be generated. In that case, this detection method should be inactivated in the grid faults. However, this method has a little fault immunity about the grid problems because of the existence of K. It is difficult to exceed the threshold for the fault detection unless severe grid problems, which can be confirmed through many simulations empirically.

III. Proposed Fault-Tolerant Control Method

An open-switch fault does not cause converter system shut-down, but its performance and reliability are slowly degraded. Therefore, a method of fault-tolerant control is proposed to solve this problem. In an ac–dc converter using SVPWM, if an open-switch fault occurs, a distorted voltage vector appears due to the inability of applying suitable voltage vectors to the PWM converter. Accordingly, the distorted voltage vector should be compensated, so that it will not cause current harmonics of the grid or fluctuations of the dc-link voltage.

A converter with a one-open-switch fault has both a healthy half cycle and an unhealthy half cycle, as shown in Fig. 2. The operation regions of the abnormal half cycle can be di-vided into single-phase condition and three-phase condition, respectively. A one-open-switch fault has two single-phase conduction regions in one cycle, as shown in Table I and Fig. 2. If single-phase control for a fault tolerance is used to mitigate a one-open-switch fault in the single-phase conduction regions, it may cause more serious distortions during the transition process

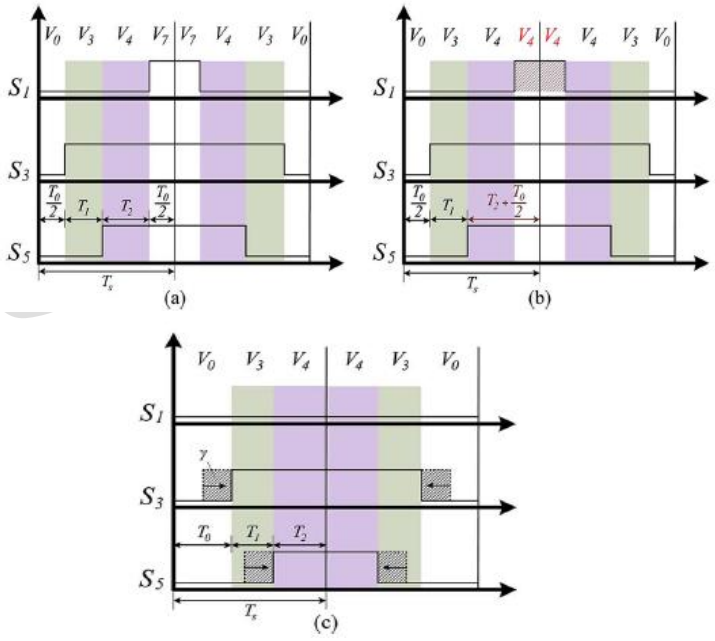

Fig. 6. Switching patterns of three operating conditions in Sec III. (a) Healthy switching patterns. (b) S_1 fault switching patterns. (c) Revised switching patterns.

from the single- to the three-phase conduction. Accordingly, during a one-open-switch fault, the single-phase control method is not recommended for the fault-tolerant control because a more serious side effect is caused. Meanwhile, in the three-phase conduction region

of the abnormal half cycle, the con-verter operates as three-phase conduction even under the faulty switch condition because the freewheeling diode of the faulty phase is turned on as in diode rectifier operation. Nevertheless, the output voltage vectors are distorted by the open-switch fault. The distorted output voltages can be divided into two cases. One is distorted only by faulted zero vectors, and the other is affected by both faulted active vectors and faulted zero vectorsIn the first case, V^{*} is implemented in Sec III of the hexagon of the SVPWM, as shown in Fig. 5. Under normal operation, the reference voltage V^{*} can be given as follows [21]–[23]:

$$V^{*} = \alpha V_n + \beta V_{n+1} + \gamma V_0 + \gamma V_7, \alpha = \frac{T_1}{T_S};\ \beta = \frac{T_2}{T_S};\ \gamma = \frac{T_0/2}{T_S} \quad (6)$$

where T_1 and T_2 are the times of the active voltage vector and T_0 is the time of the zero vector. n is the nth sector number in Fig. 5. In general, V_0 and V_7 have switching times with the same duration because the symmetric PWM is used to reduce the current ripple [21].

Fig. 6(a) shows the switching patterns in Sec III for healthy operation. The voltage vectors in Sec III include active vectors V_3 and V_4 and zero vectors V_0 and V_7, as can be seen in (6) and Fig. 6(a). If there is an S_1 switch open fault, the zero vector V_7(1, 1, 1) is converted into an active vector V_4(0, 1, 1)as shown in Fig. 6(b). The faulted output voltage $V_{\text{fault1}}{}^{S1}$ caused by an S_1 switch failure can be expressed as follows

$$V_{\text{fault1}}{}^{S1} = \alpha V_3 + \beta V_4 + \gamma V_0 + \gamma V_4.$$

This vector is only distorted by the zero vector.

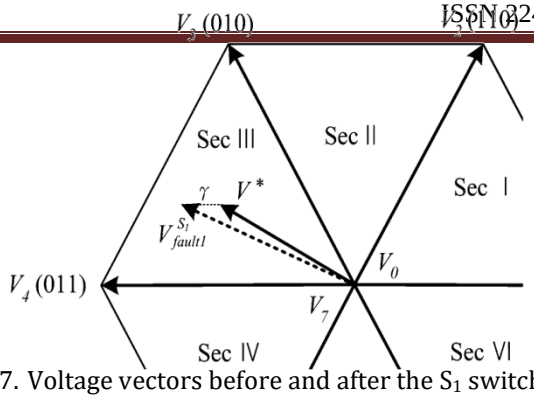

Fig. 7. Voltage vectors before and after the S_1 switch open fault in Sec III.

where V_{zero} is the zero vector and $V_{\text{zero}}{}^{f}$ is the faulted zero vector after the failure. Table II shows the voltage vector components before and after a fault by considering the six fault cases of the switching elements. If the S_1 switch is faulty as in the previous example, $V_{\text{zero}}{}^{f}$ is V_4 which is changed from V_7, under the condition of $i_a < 0$ from Table II. As a result, the voltage expression in Sec III is equal to (7). If the three-phase ac–dc PWM converter has an arbitrary switch with an open fault, the faulted voltage vector can be expressed by using (8) and Table II in the case of being distorted by one zero vector. Fig. 8(a) shows the healthy switching patterns of V^{*} in Sec II in the second case. The voltage vector consists of active vectors V_2 and V_3 and zero vectors as in (6). If an S_1 fault occurs, the active vector V_2(1, 1, 0) and the zero vector V_7(1, 1, 1) are converted into the active vector V_3(0, 1, 0) and the active vector V_4(0, 1, 1), respectively, as shown in Fig. 8(b). The faulted output voltage vector $V_{\text{fault2}}{}^{S1}$ is obtained in the following:

$$V_{\text{fault2}}{}^{S1} = \alpha V_3 + \beta V_3 + \gamma V_0 + \gamma V_4. \quad (9)$$

This vector is affected by both zero vectors and one active vector. In (9), this second fault case is defined as *fault2* and used as a subscript. Fig. 9 shows the voltage vectors before and after an S_1 fault in Sec II. The fault voltage vector is shifted by

Fault switch	Condition	Zero vector		Active vector			
		Before(V_{zero})	After(V_{zero}^{f})	Before(V_n)	After(V_{active})	Before(V_{n+1})	After(V_{active})
S_1(A Top)	if (ia<0)	V_7(111)	V_4(011)	V_2(110)	V_3(010)	V_6(101)	V_5(001)
S_2(C Bot)	if (ic>0)	V_0(000)	V_5(001)	V_3(010)	V_4(011)	V_1(100)	V_6(101)
S_3(B Top)	if (ib<0)	V_7(111)	V_6(101)	V_4(011)	V_5(001)	V_2(110)	V_1(100)
S_4(A Bot)	if (ia>0)	V_0(000)	V_1(100)	V_5(001)	V_6(101)	V_3(010)	V_2(110)
S_5(C Top)	if (ic<0)	V_7(111)	V_2(110)	V_6(101)	V_1(100)	V_4(011)	V_3(010)
S_6(B Bot)	if (ib>0)	V_0(000)	V_3(010)	V_1(100)	V_2(110)	V_5(001)	V_4(011)

Fault switch	Condition	Zero vector		Active vector			
		Before(V_{zero})	After(V^{f}_{zero})	Before(V_n)	After(V_{active})	Before(V_{n+1})	After(V_{active})
S_1(A Top)	if (ia<0)	V_7(111)	V_4(011)	V_2(110)	V_3(010)	V_6(101)	V_5(001)
S_2(C Bot)	if (ic>0)	V_0(000)	V_5(001)	V_3(010)	V_4(011)	V_1(100)	V_6(101)
S_3(B Top)	if (ib<0)	V_7(111)	V_6(101)	V_4(011)	V_5(001)	V_2(110)	V_1(100)
S_4(A Bot)	if (ia>0)	V_0(000)	V_1(100)	V_5(001)	V_6(101)	V_3(010)	V_2(110)
S_5(C Top)	if (ic<0)	V_7(111)	V_2(110)	V_6(101)	V_1(100)	V_4(011)	V_3(010)
S_6(B Bot)	if (ib>0)	V_0(000)	V_3(010)	V_1(100)	V_2(110)	V_5(001)	V_4(011)

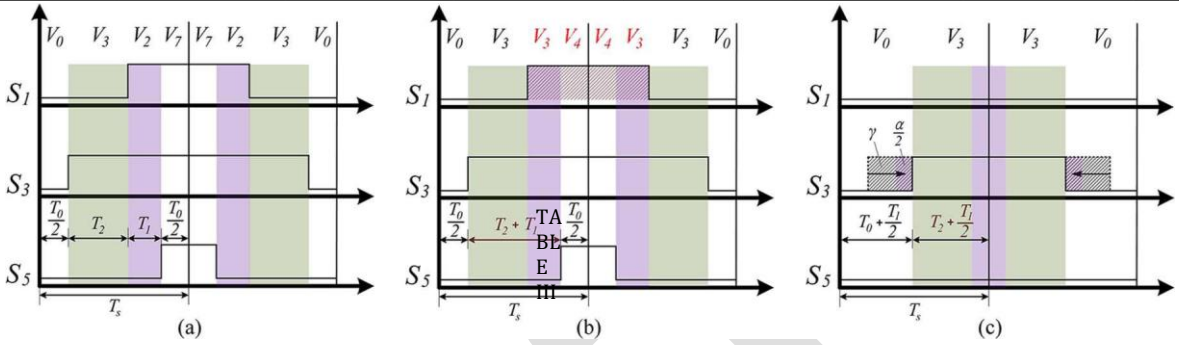

TABLE III

faulted and compensated output voltage vectors of one cycle under the s_1 switch open-fault condition

Healthy condition			Faulty condition		Fault tolerant control	
Sector	Vectors	a-phase current sign	Vectors and switching time	faulted vector	Vectors and switching time	Compensation performance
SecI	V_0, V_1, V_2, V_7	(+)	$V_0(T_0/2), V_1(T_1), V_2(T_2), V_7(T_0/2)$	*Nothing*	Not required	
SecII	V_0, V_2, V_3, V_7	(+)	$V_0(T_0/2), V_2(T_1), V_3(T_2), V_7(T_0/2)$	*Nothing*	Not required	
		0	Single-phase conduction region		Uncontrollable	
		(-)	$V_0(T_0/2), V_3(T_1+T_2), V_4(T_0/2)$	*zero, active*	$V_0(T_0), V_3(T_1/2+T_2)$	*partially*
SecIII	V_0, V_3, V_4, V_7	(-)	$V_0(T_0/2), V_3(T_1), V_4(T_2+T_0/2)$	*zero*	$V_0(T_0), V_3(T_1), V_4(T_2)$	*perfectly*
SecIV	V_0, V_4, V_5, V_7	(-)	$V_0(T_0/2), V_5(T_1), V_4(T_2+T_0/2)$	*zero*	$V_0(T_0), V_5(T_1), V_4(T_2)$	*perfectly*
SecV	V_0, V_5, V_6, V_7	(-)	$V_0(T_0/2), V_5(T_1+T_2), V_4(T_0/2)$	*zero, active*	$V_0(T_0), V_5(T_1+T_2/2)$	*partially*
		0	Single-phase conduction region		Uncontrollable	
		(+)	$V_0(T_0/2), V_5(T_1), V_6(T_2), V_7(T_0/2)$	*Nothing*	Not required	
SecVI	V_0, V_6, V_1, V_7	(+)	$V_0(T_0/2), V_6(T_1), V_1(T_2), V_7(T_0/2)$	*Nothing*	Not required	

In the *fault2* case of being distorted by both zero and active vectors as in (9), perfect compensation is impossible because one active vector V_2 is not available due to the faulty switch. However, the voltage vector can be partially compensated by using vector projection, as shown in Fig. 11. If the reference voltage vector V^{*} is projected orthogonally onto the other active vector V_3, it is the nearest available voltage vector based on the reference voltage vector. An equilateral triangle with the three equal sides of α is shown in Fig. 9, which is made by the peak point of V^{*} and on the line of V_3. Orthogonal projection of the reference vector divides side α in half on the V_3 axis, as shown in Fig. 11. Therefore, the faulted voltage vectors in (9) and (10) can be updated into the following for the compensation:

$$V_{\text{compen2}}^{S_1} = (\alpha/2 + \beta)V_3 + (\alpha/2 + 2\gamma)V_0 \quad (13)$$

$$V_{\text{compen2}} = (\alpha/2 + \beta)V_{\text{active}} + (\alpha/2 + 2\gamma)V_{\text{zero}}. \quad (14)$$

γV_4 in (9) is replaced with γV_0, and $\alpha V_3/2$ is exchanged with $\alpha V_0/2$ to get the closest vector of the voltage vector reference, as shown in (13). The revised switching pattern is shown in Fig. 8(c). The general compensation expression can be acquired like (14). In this *compen2* case, the proposed method improves the current response by using the closest voltage vector.

Table III shows the faulted and compensated output voltage vectors under the S_1 switch open-fault condition according to the switching patterns of SVPWM and the directions of a faulty phase current. Despite the fault, the positive half cycle is healthy because an upper switch fault does not affect the positive current flow of the faulty phase in a three-phase ac–dc PWM converter. Hence, when the S_1 switch is faulty (Sec I and Sec VI), the parts of Sec II and Sec V are not related to the failure of S_1 so that there is no faulted vector ("nothing" in Table III) and compensations

are not required. However, if the *a*-phase current is less than zero, the output voltage vectors are distorted. The negative half cycle can be divided into the single-phase conduction regions and the unhealthy three-phase conduction regions. Two single-phase conduction regions are the detection regions in Table I. In these regions, fault detection is possible, but tolerance control is impossible due to a more serious side effect as mentioned earlier. In the remaining unhealthy three-phase conduction regions, the distorted output voltage vectors can be compensated partially or perfectly by

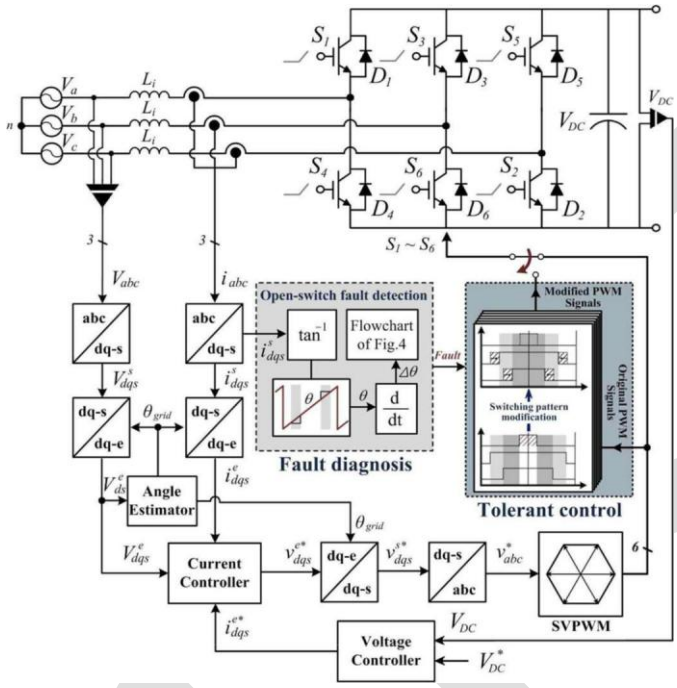

Fig. 12. Block diagram of the proposed fault-tolerant control of a three-phase ac–dc PWM converter.

Table IV

Experimental Parameters

Input voltage	3Φ 220[V]	Grid input frequency	60[Hz]
Input Reactor	5[mH]	DC-link capacitor	2,350[uF]
DC Reference voltage	400[V]	Load power	1[kW]
Switching frequency	5[kHz]	PWM method	SVPWM

using the proposed method. The faulty and compensated output voltage vectors in Sec II and Sec III are like (7), (9), (11), and (13). Likewise, the voltage vectors in Sec IV and Sec V will be obtained by using the same method In heavy load, the phase angle difference between the con-verter and grid voltage is increased to obtain the large currents. It causes that the dwell time of the partial compensation region in Sec II is increased by approaching the voltage reference vector toward the active vector V_2. Therefore, the compensation performance is a little degraded in the higher load. However, this compensation method works effectively for all load levels because the impact of the degradation is insignificant.

In the grid-connected ac–dc PWM converter, the modulation index is related to the dc-link voltage. The higher the dc-link voltage, the lower the Modulation index. In the low modulation, because the zero vector time T_0 is longer than that in high modulation, the voltage vector is distorted more seriously in the open-switch fault condition. Hence, the current distortion and dc-link voltage ripple are more deteriorated. However, this compensation method is effective equally regardless of the PWM.

Fig. 12 shows the entire block diagram of a three-phase ac–dc PWM converter including the proposed fault detection and fault-tolerant control methods. In Fig. 12, the fault diagnosis uses the measured three phase currents to get the current phase angle. Then, from the variation of the current angle, the fault and the faulty switch can be determined. When an open-switch fault is detected, the proposed fault-tolerant control method is activated and makes the PWM switching pattern modified to get the compensated voltage vector. There are six kinds of switch-ing patterns according to the six fault switches. The modified PWM switching signal is selected instead of the unavailable original signal in several regions including the distorted voltage vector.

The proposed fault-tolerant control method can reduce the imbalance of the three phase currents by using modified PWM switching signals. Hence, the dc-link voltage ripple of the converter is reduced.

IV. EXPERIMENTAL RESULT

Experiments have been performed to verify the proposed diagnosis and fault-tolerant control methods. Table IV shows the experimental parameters of the PWM converter system.

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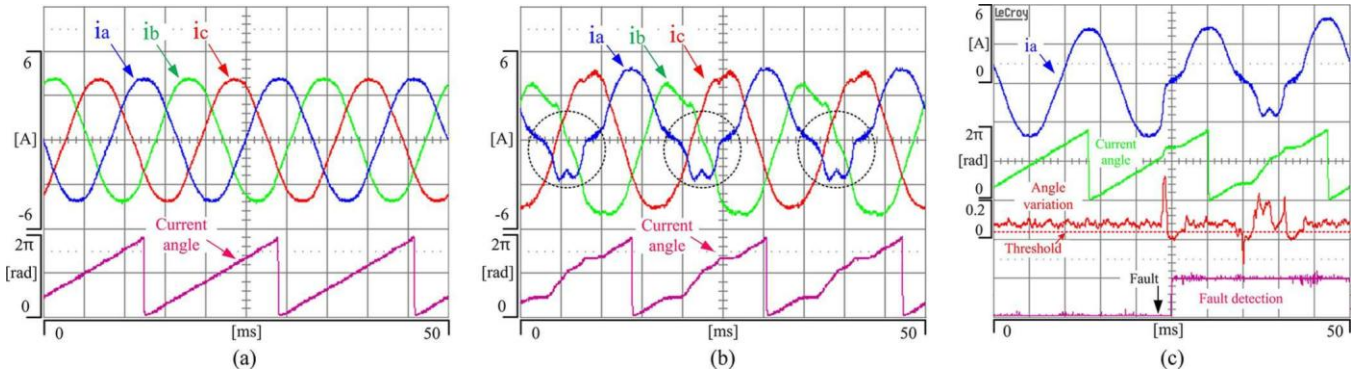

Fig. 13. Experimental results for the fault detection.

(a) Healthy condition. (b) S_1 switch faulty condition.

(c) Detection signal before and after the fault.

Fig. 13 shows the experimental results for the fault detection. Fig. 13(a) shows the three phase currents and the current angle under the healthy condition. Low-pass filters of second order with 10-kHz cutoff frequency are used in the input of the analog-to-digital converter for current measurement to reduce the effect of the switching noise [26]. The phase currents are acquired at the middle point of SVPWM per every sampling time from the current sensors and shown through the digital-to- analog converter [27]. Hence, the currents are almost sinusoidal waveforms with no distortion. The three phase currents have balanced sine waveforms so that the current angle rotates constantly. If an S_1 switch open fault occurs in the PWM converter, the waveforms in Fig. 13(a) are changed into those in Fig. 13(b), as shown in Fig. 2. As mentioned earlier, the neg-ative current of the *a* phase is distorted and the *b*- and *c*-phase currents are affected during the unhealthy half cycle, as shown in the three circles in Fig. 13(b). The distorted three phase currents directly affect the distorted current angle, as shown in Fig. 13(b). Fig. 13(c) shows the *a*-phase current, the current angle, the variation of the current angle, and the fault detection signal before and after the S_1 switch fault. Before the fault, the *a*-phase current and the current angle are healthy waveforms as in Fig. 13(a). In this case, the variation of the current angle is kept constant because the current angle is constantly increasing. Hence, the variation is always higher than the threshold value in the healthy condition, as shown in Fig. 13(c). However, after the S_1 fault, the *a*-phase current and the current angle are distorted. Thus, the variation of the current angle is not kept constant during the unhealthy half cycle. The variation is lower than the threshold value in the single-phase conduction region. Thus, the fault detection signal can be obtained by using the flowchart algorithm in Fig. 4.

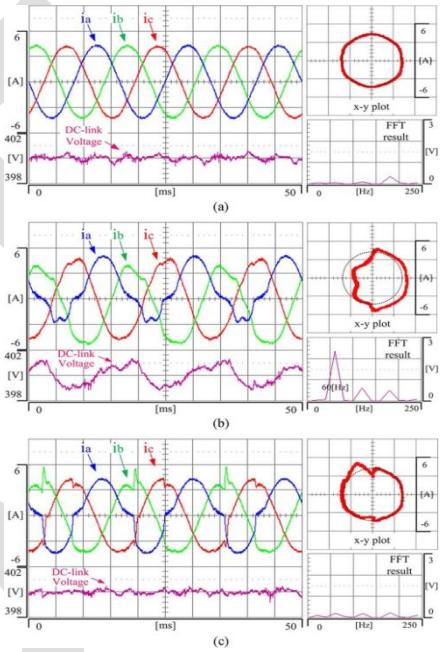

Fig. 14 shows the three phase currents, the dc-link voltage, the fast Fourier transform (FFT) result of the dc-link voltage, and the *x*–*y* plot of the three phase currents

under the three operating conditions. In the healthy condition, the three phase currents are balanced so that the current trajectory on the *x*–*y* plot is a perfect circle. Hence, the dc-link voltage is flat without a voltage ripple, as shown in Fig. 14(a). How-ever, if an S_1 switch fault occurs, unbalanced three phase currents, including harmonics, are generated. Thus, the cur-rent trajectory is distorted on the left half plane of the *x*–*y* plot, as shown in Fig. 14(b). As a result, the dc-link voltage fluctuates with the grid frequency (60 Hz). If the proposed fault-tolerant control is applied after a fault is detected, the current imbalance and the dc-link voltage ripple are noticeably reduced, as shown in Fig. 14(c). The peak of the *b*-phase current is made to get quickly the healthy current at the end of the single-phase conduction. In the *x*–*y* plot in Fig. 14(c), the current trajectory is similar to the circle in the healthy condition except for the single-phase conduction regions. This means that

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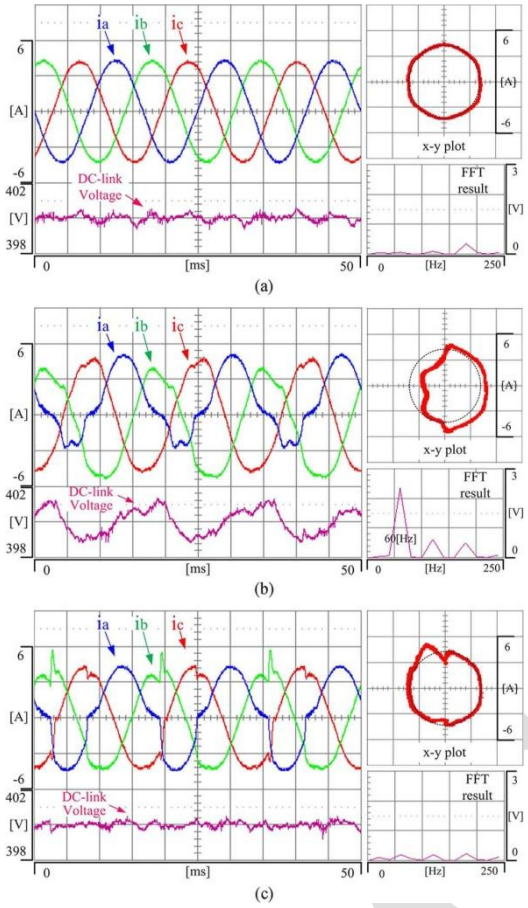

Fig. 15. Three phase currents, dc-link voltage, FFT result of the dc-link voltage, and *x–y* plot of the three phase currents. (a) Healthy condition. (b) S_1 switch open-fault condition. (c) Proposed fault-tolerant control operation

the dc-link voltage fluctuation and the harmonics of the input current are considerably reduced by using the proposed fault-tolerant control method. Table V shows the numerical results in Fig. 14, the current's total harmonic distortion (THD), and the power factors under the three operating conditions.

V. CONCLUSION

This paper has analyzed one-open-switch fault cases and pro-posed both fault diagnosis and fault-tolerant control methods for open-switch failures in three-phase ac–dc PWM converters. If an open-switch fault occurs in a converter, the performance and reliability can be degraded. The faulty switch can be found by observing the variation of the current angle obtained from the measured three phase currents. The proposed fault-tolerant control method can improve the performance and the reliability by modifying the PWM switching patterns when a fault is detected. Hence, the dc-link voltage ripple is reduced, and the

TABLE V

Numerical Results Under The Three Operating Conditions

		Healthy condition		Faulty condition		Tolerance control	
		Magnitude [A]	THD [%]	Magnitude [A]	THD [%]	Magnitude [A]	THD [%]
Current	A phase	4.022	1.28	3.347	22.87	3.88	18.82
	B phase	4.022	1.28	4.361	12.07	3.991	9.38
	C phase	4.028	1.28	4.618	11.54	4.056	9.81
DC-link voltage ripple		(p-p) 0.2[V]		(p-p) 2[V]		(p-p) 0.3[V]	
Power factor		Nearly 1		0.94		0.973	

efficiency and power factor are also improved. This method is easily implemented without any additional H/W by modifying PWM switching times using software. The usefulness of the proposed method was verified through experimental results.

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