Carry Select Adder – Review

Gagandeep Singh Gill\(^1\), Chakshu Goel\(^2\)

\(^1\) Department of Electronics and Communication Engineering, SBSSTC, Ferozepur, Punjab, India, +919464526267.
\(^2\) Department of Electronics and Communication Engineering, SBSSTC, Ferozepur, Punjab, India, +918427688795.

ABSTRACT

To perform fast addition operation, CSLA is one of the fastest adders used in many data-processing processors. There is further scope of improving the performance parameters of CSLA. This paper provides a comparative analysis of CSLA and reviews about various proposed schemes used to reduce the delay time, area occupied and power consumption in CSLA.

Keywords: Carry Select Adder, Ripple Carry Adder, Delay, Area occupied, Power consumption

INTRODUCTION

Digital adders are important part of computers and other kind of processors. Adders perform the operation of addition of numbers. Adders are used in arithmetic and logic unit (ALU), for calculating addresses in processor and various biomedical applications. One of the main applications of adders is to execute various transform algorithms like FFT, IIR and FIR in digital signal processing. So now days, a research is being carried out to design an adder circuit with low power consumption and having lesser area and delay time. The delay time in digital adders is proportional to the time taken by the carry signal to propagate through the adder. Depending on this carry propagation time, the various types of adder are Ripple Carry Adder (RCA), Carry Look Ahead Adder and Carry Select Adder (CSLA). RCA consists of full adders cascaded in series. This type of adder is not efficient because the delay time is more and delay increases with the increase in number of bits used for addition. Time critical applications require the use of Carry Look Ahead adder as in this type of adder additional circuitry is used to generate carry bits in parallel but this increases the circuit complexity and area occupied. The CSLA provides a compromise between area consumption and delay time of adder [1] [2].
Table 1. Comparison of various Adder’s

<table>
<thead>
<tr>
<th>Adder</th>
<th>Delay</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple Carry adder</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Carry Select adder</td>
<td>(\sqrt{N})</td>
<td>2N</td>
</tr>
<tr>
<td>Carry Look Ahead adder</td>
<td>(\log N)</td>
<td>(N^3)</td>
</tr>
</tbody>
</table>

This paper presents a review of Carry Select Adder (CSLA) and tells about the research work done in the field of CSLA since from its introduction. This paper is organised as follows: In section II comparative analysis of CSLA is shown and section III deals with conclusion.

**COMPARATIVE ANALYSIS OF CSLA**

In digital adders, the delay time is proportional to the time taken by a carry to propagate through the adder. The sum for each bit position requires a carry from previous stage. The worst case delay for RCA is shown in fig 1. This problem of carry propagation delay is mitigated by using CSLA.

![Fig 1: Worst case delay in 4-bit RCA](image)

CSLA consists of pair of blocks of RCA for addition i.e. one block of RCA with \(C_{in}(\text{carry in}) = 0\) and other block of RCA with \(C_{in} = 1\). The correct sum output is selected depending on the value of previous stage carry and thus speed of addition is increased. 4-bit CSLA is shown in fig 2.[1].

![Fig 2: 4-bit Carry Select Adder](image)
A typical CSLA discussed earlier uses a pair of carry evaluation blocks, one with carry in of 0 and other with carry in of 1 which causes the more area consumption. A. Tyagi proposed a new scheme in which single carry evaluation block with Cin= 0 was sufficient and results of carry evaluation block with Cin= 1 can be derived from Cin= 0 block with little extra logic. This resulted in decrease in area consumption and delay time [2].

Further T.Y. Chang published a paper and the proposed CSLA had better performance. In this scheme, an add-one circuit was introduced which replaced the RCA with Cin= 1 present in typical CSLA. The multiplexer was used to produce the correct sum output. The add-one circuit used was based on the complement scheme. The complement scheme states that if Sn^1 and Sn^0 be sum outputs of two RCA’s with Cin= 1 and Cin= 0 respectively then Sn^1 can be generated by inverting each Sn^0 bit starting from LSB until the first zero is found. In this paper, instead of using Full adders for RCA block with Cin= 0, Half adders are used. This helped in reducing the number of transistors used and thus reducing the area occupied but at the slight cost of speed of addition. [3] [4].

R. Hashermian put forward an algorithm to make CSLA as more area efficient and having quick response time. In this algorithm input operands are divided into fine slices and carries were produced in groups rather than individually. Therefore the carries within a group were generated at the same time and also the number of carries in each group was equal to those already generated. This caused the exponential growth in generation of carries which reduced the overall delay time of CSLA [5].

Then a new technique known as pipelining came into consideration and Y. Kim designed a pipelined CSLA to achieve high data rate. A pipelined CSLA using the complementary scheme was proposed. In this scheme, 32-bit pipelined adder was made combining four smaller block adders that operate in parallel. This proposed adder resulted in lesser area and power consumption [10].

Further enhancement was done in CSLA by designing CSLA based on compact Carry Look-Ahead unit. The Carry Look-Ahead unit had compact, static and multi-output structure with less number of transistors and the new selection circuit was used which was based on NMOS pass transistors. This modification resulted in reduction in area and dynamic power of CSLA[11].

All the CSLA schemes discussed earlier are linear i.e. speed of CSLA is linearly proportional to bit length used for addition. But to optimise the worst case delay of CSLA, square root scheme was introduced by Y. He. In this scheme, block size of RCA in CSLA is selected such that arrival time of sum signal at the multiplexer optimally matches with the delay time of carry in signal (as select signal at MUX). The proposed square root CSLA had a power-delay and area-delay performance improvement [12].
In a recent research done on CSLA, an add-one circuit was modified to improve performance of adder. In this proposed square root CSLA, Binary to Excess-1 converter (BEC) was used as an add-one circuit. The 4-bit Binary to Excess-1 converter is shown in figure 3. This BEC logic resulted in large silicon area reduction and power consumption when designing higher bit CSLA’s. But this reduction in area was at the cost of slight increase in delay [13].

CONCLUSION

Power, delay and area are the main performance parameters of CSLA and the reduction of these parameters is the challenging issue of today’s VLSI research. Many schemes have been proposed to design fast, compact and less power consuming CSLA. But as we can analyze from the recent scheme proposed that there is a trade-off between area consumption and delay of CSLA. Therefore there is a scope to make CSLA more delay and area efficient. Other parameters like frequency, number of gate clocks, length etc. can be optimized.

REFERENCES


